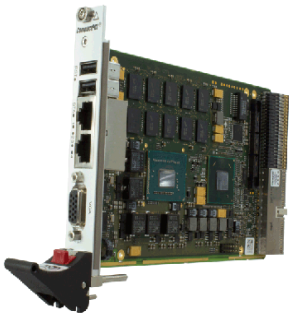
# User Manual

# F22P – 3U CompactPCI® PlusIO Intel® Core™ i7 CPU Board



# F22P - 3U CompactPCI® PlusIO Intel® Core™ i7 CPU Board

The F22P versatile 4HP/3U single-board computer is a continuation of MEN's proven range of Intel® CPU boards. It is equipped with the high-performance third generation Intel® Core™ i7 processor running at up to 3.3 GHz maximum turbo frequency and offering the latest quad core processor architecture from Intel® with full 64-bit support. The CPU card delivers an excellent graphics performance and is designed especially for embedded systems which require high computing performance with low power consumption.

The F22P offers a 32-bit/33-MHz CompactPCI® bus interface and can also be used without a bus system. 4 USB 2.0 ports, 4 PCI Express® x1 links, 2 SATA 3 Gb/s and 2 SATA 6 Gb/s interfaces as well as one Gigabit Ethernet are led to the J2 rear I/O connector which is compatible with the PICMG 2.30 CompactPCI® PlusIO specification.

The F22P is equipped with a state-of-the-art fast DDR3 DRAM which is soldered to the F22P to guarantee optimum shock and vibration resistance. An mSATA disk and a microSD™ card device which are connected via a USB interface and a SATA channel offer nearly unlimited space for user applications.

The standard I/O available at the front panel of F22P includes graphics on a VGA connector, two PCIe®-driven Gigabit Ethernet as well as two USB 2.0 ports.

The F22P can be extended by different side cards. Additional functions include a digital video interface for flat panel connection via DVI (multimedia), a variety of different UARTs or another four USBs, SATA for hard disk connection and HD audio.

Thermal supervision of the processor and a watchdog for the operating system complete the functionality of the F22P. A TPM (Trusted Platform Module) chip is also assembled.

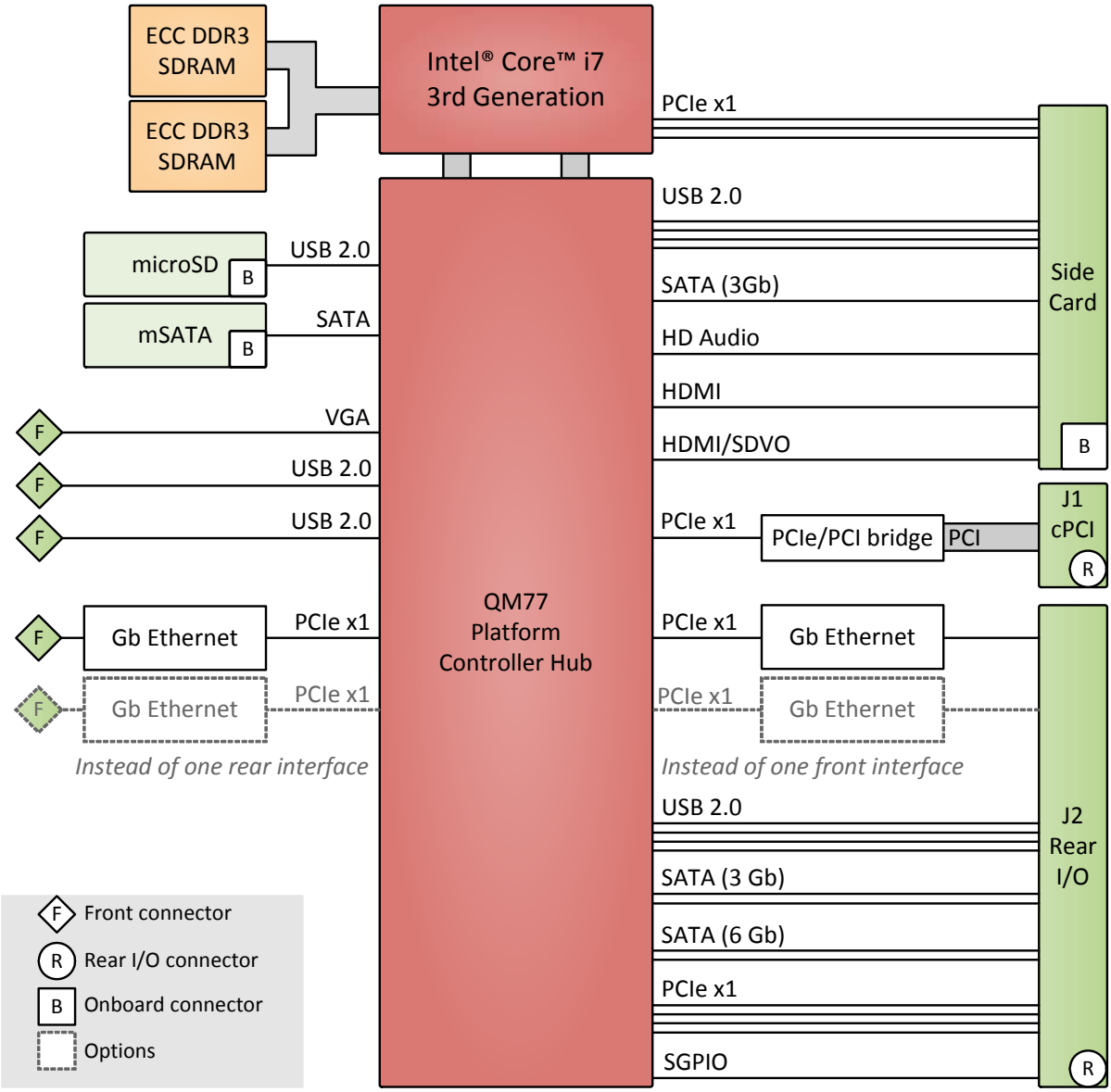
The F22P operates in Windows® and Linux environments as well as under real-time operating systems that support Intel®'s multi-core architecture. The InsydeH2O™ EFI BIOS was specially designed for embedded system applications.

Equipped with Intel® components exclusively from the Intel® Embedded Line, the F22P has a guaranteed minimum standard availability of 7 years.

The F22P is suited for a wide range of industrial applications, e.g. for monitoring, vision and control systems as well as test and measurement. Main target markets comprise industrial automation, multimedia, traffic and transportation, aerospace, shipbuilding, medical engineering and robotics.

The F22P comes with a tailored passive heat sink within 4 HP height. The robust design of the F22P makes the board especially suited for use in rugged environments with regard to shock and vibration according to applicable DIN, EN or IEC industry standards. The F22P is also ready for coating so that it can be used in humid and dusty environments.

# Diagram


ECC DDR3 SDRAM
ECC DDR3 SDRAM
Intel® Core™ i7 3rd Generation
PCIe x1
USB 2.0
SATA (3Gb)
HD Audio
HDMI
HDMI/SDVO
Side Card
B
microSD
B
USB 2.0
mSATA
B
SATA
VGA
F
USB 2.0
F
USB 2.0
F
PCIe x1
PCIe/PCI bridge
PCI
J1 cPCI
R
QM77 Platform Controller Hub
F
Gb Ethernet
PCIe x1
F
Gb Ethernet
PCIe x1
Instead of one rear interface
PCIe x1
Gb Ethernet
PCIe x1
Gb Ethernet
Instead of one front interface
USB 2.0
SATA (3 Gb)
SATA (6 Gb)
PCIe x1
SGPIO
J2 Rear I/O
R
F Front connector
R Rear I/O connector
B Onboard connector
Options

# Technical Data

### CPU

- Intel® Core™ i7-3615QE
  - 2.3 GHz processor core frequency
  - 3.3 GHz maximum turbo frequency
  - 1066 MHz system bus frequency
- Chipset
  - QM77 Platform Controller Hub (PCH)

### Memory

- Up to 6 MB last level cache integrated in i7
- Up to 16 GB SDRAM system memory
  - Soldered
  - DDR3 with ECC support
  - 1066/1333/1600 MHz memory bus frequency
- 64 Mbits boot Flash
- Serial EEPROM 2kbits for factory settings

### Mass Storage

- microSD™ card interface
  - Connected via one USB port
- mSATA disk slot
  - Connected via one SATA channel
- Serial ATA (SATA)
  - Four channels via rear I/O, one channel via side-card connector, one channel for mSATA disk
  - 4 SATA 3 Gbit/s interfaces, 2 SATA 6 Gbit/s interfaces (rear I/O)
  - RAID level 0/1/5/10 support

### Graphics

- Integrated in QM77 chipset
  - 650 MHz graphics base frequency
  - 1.2 GHz graphics maximum dynamic frequency
- VGA connector at front panel
- Two digital display interface ports available via side-card connector
  - DisplayPort®, HDMI and SDVO (SDVO only on one interface)
  - One additional DVI connector at front panel optional via side card
  - Simultaneous connection of two monitors

### I/O

- USB
  - Two USB 2.0 ports via Series A connectors at front panel
  - Four USB 2.0 ports via side-card connector
  - Four USB 2.0 ports via rear I/O
  - One USB for connection of microSD
  - EHCI implementation
  - Data rates up to 480 Mbit/s
- Ethernet
  - Two 10/100/1000Base-T Ethernet channels at the front
  - RJ45 connectors at front panel
  - Ethernet controllers are connected by two x1 PCIe® links
  - LEDs to signal activity status and connection speed
  - One 10/100/1000Base-T Ethernet channel via rear I/O
  - Ethernet controller is connected by one x1 PCIe® link
- High Definition (HD) audio
  - Accessible via side-card connector

### Front Connections (Standard)

- VGA
- Two USB 2.0 (Series A)
- Two Ethernet (RJ45)

### Rear I/O (PICMG 2.30)

- Four SATA
- Four USB
- One Gigabit Ethernet (second rear interface instead of one front interface as an assembly option)
- Four PCI Express® x1 links
- Compatible with PICMG 2.30 CompactPCI® PlusIO
  - 1PCI33/4PCIE5/2SATA3/2SATA6/4USB2/1(2)ETH1G

### Miscellaneous

- Board controller
- Real-time clock, buffered by a GoldCap or alternatively a battery (5 years life cycle)
- Watchdog timer
- Temperature measurement
- One user LED
- Reset button

### PCI Express

- Three x1 links to connect local 1000Base-T Ethernet controllers
  - Data rate 250 MB/s in each direction (2.5 Gbit/s per lane)
- Four x1 links via rear I/O
  - Data rate up to 500 MB/s in each direction (5 Gbit/s per lane)
- Three x1 links for extension through side-card connector
  - Data rate up to 500 MB/s in each direction (5 Gbit/s per lane)

### CompactPCI® Bus

- Connection via PCI Express® link from processor using PCI-Express-to-PCI-Bridge
- Compliance with CompactPCI® Core Specification PICMG 2.0 R3.0
- System slot
- 32-bit/33-MHz CompactPCI® bus
- V(I/O): +3.3V (+5V tolerant)

### Busless Operation

- Board can be supplied with +5V only, all other voltages are generated on the board
- Backplane connectors used only for power supply

### Electrical Specifications

- Supply voltage/power consumption (board versions with i7-2715QE processor)
  - +5V (-3%/+5%), 9.6 A typ., 14.4 A max.
  - +3.3V (-3%/+5%), 1.8 A (3 Gb Ethernet), 1.4 A (2 Gb Ethernet), 1 A (1 Gb Ethernet)
  - +12V (-10%/+10%), approx. 10 mA
  - If the board is supplied with 5V only (typically without a bus connection), the 3.3V are generated on the board and fed to the backplane (3A max.) No external 3.3 V voltage may be applied in that case!

### Mechanical Specifications

- Dimensions: conforming to CompactPCI® specification for 3U boards
- Front panel: 4HP with ejector
- Weight: 204 g (w/o heat sink)

### Environmental Specifications

- Temperature range (operation):
  - Depends on system configuration (CPU, hard disk, heat sink...)
  - Maximum: +85°C
  - Minimum: -40°C (all processors)
  - Conditions: airflow 1.5m/s, typical power dissipation: 12 W (board versions with i7-2715QE processor) with Windows® XP operating system and 1 Gb Ethernet connection
- Temperature range (storage): -40..+85°C
- Relative humidity (operation): max. 95% non-condensing
- Relative humidity (storage): max. 95% non-condensing
- Altitude: -300m to + 2,000m
- Shock: 50 m/s², 30 ms
- Vibration (Function): 1 m/s², 5 Hz – 150 Hz
- Vibration (Lifetime): 7.9 m/s², 5 Hz – 150 Hz
- Conformal coating on request

### MTBF

- 549 414 h @ 40°C according to IEC/TR 62380 (RDF2000)

### Safety

- PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers

### EMC

- Tested according to EN 55022 (radio disturbance), IEC 61000-4-3 (electromagnetic field immunity), IEC 61000-4-4 (burst) and IEC 61000-4-6 (conducted disturbances)

### BIOS

- InsydeH2O™ UEFI Framework

### Intel® Active Management Technology

- Manageability Engine in Chipset
- Network Filters in Chipset
- Dedicated Flash Storage Area
- Out of Band (OOB) Access
  - Power off Access
  - Independent of OS status
  - Power status control
  - Keyboard-Video-Mouse (KVM) Viewer (VNC-compatible)
  - IDE-Redirect
  - Serial-over-LAN

### Software Support

- Note that 64-bit hardware technology can be used in an optimal way with 64-bit operating system support
- Windows
- Linux
- VxWorks® (on request)
- QNX® (on request)
- Intel® Virtualization Technology, allows a platform to run multiple operating systems and applications in independent partitions; one computer system can function as multiple "virtual" systems.

For more information on supported operating system versions and drivers, please see the online data sheet.

# Configuration Options

### CPU

- Intel® Core™ i7-3615QE
  - Quad Core, 2.3 GHz, 6 MB Cache, 45 W
- Intel® Core™ i7-3612QE
  - Quad Core, 2.1 GHz, 6 MB Cache, 35 W
- Intel® Core™ i7-3555LE
  - Dual Core, 2.5 GHz, 4 MB Cache, 25 W
- Intel® Core™ i7-3517UE,
  - Dual Core, 1.7 GHz, 4 MB Cache, 17 W
- Intel® Core™ i5-3610ME
  - Dual Core, 2.7 GHz, 3 MB Cache, 35 W
- Intel® Core™ i3-3120ME
  - Dual Core, 2.4 GHz, 3 MB Cache, 35 W
- Intel® Core™ i3-3217UE
  - Dual Core, 1.6 GHz, 3 MB Cache, 17 W
- Intel® Celeron® 1020E
  - Dual Core, 2.2 GHz, 2 MB Cache, 35 W
- Intel® Celeron® 1047UE
  - Dual Core, 1.4 GHz, 2 MB Cache, 17 W
- Intel® Celeron® 927UE (without PCI Express® on side card)
  - Single Core, 1.5 GHz, 1 MB Cache, 17 W

### Memory

- System RAM
  - Up to 16 GB
- microSD™ card
  - 0 MB up to maximum available
- mSATA disk
  - 0 MB up to maximum available

### Graphics

- One DVI-D connector at front via side card
  - Simultaneous connection of two monitors

### I/O

- Ethernet
  - 9-pin D-Sub connector with one or two 10/100Base-T ports instead of two RJ45 connectors
  - Second Ethernet at rear I/O connector J2 instead of one interface at the front
- Rear I/O
  - VGA on CompactPCI® J2 connector as an assembly option for the conduction-cooled board version
  - VBATT on CompactPCI® J1 connector as an assembly option for the conduction-cooled board version

### Mechanical

- Side card can be added at left or right side of CPU

### Operating Temperature

- Depends on system configuration (CPU, hard disk, heat sink...)
- Maximum: +85°C
- Minimum: -40°C (all processors)

### Cooling Concept

- Also available with conduction cooling in MEN CCA frame

### Software Support

- VxWorks® (on request)
- QNX® (on request)

**Please note that some of these options may only be available for large volumes. Please ask our sales staff for more information.**

For available standard configurations see the online data sheet.

# Product Safety

## Lithium Battery

This board contains a lithium battery. There is a danger of explosion if the battery is incorrectly replaced!

Please see Chapter 4 Maintenance on page 78

## Electrostatic Discharge (ESD)

Computer boards and components contain electrostatic sensitive devices. Electrostatic discharge (ESD) can damage components. To protect the board and other components against damage from static electricity, you should follow some precautions whenever you work on your computer.

- Power down and unplug your computer system when working on the inside.
- Hold components by the edges and try not to touch the IC chips, leads, or circuitry.
- Use a grounded wrist strap before handling computer components.
- Place components on a grounded antistatic pad or on the bag that came with the component whenever the components are separated from the system.
- Only store the board in its original ESD-protected packaging. Retain the original packaging in case you need to return the board to MEN for repair.

# About this Document

This user manual is intended only for system developers and integrators, it is not intended for end users.

It describes the hardware functions of the board, connection of peripheral devices and integration into a system. It also provides additional information for special applications and configurations of the board.

The manual does not include detailed information on individual components (data sheets etc.). A list of literature is given in the appendix.

## History

| Issue | Comments | Date |
|---|---|---|
| E1 | First issue | 2013-08-20 |
| E2 | Corrected options and minor errors, added RTC accuracy, reworked block diagram, cosmetics | 2015-01-15 |

## Conventions

Indicates important information or warnings concerning proper functionality of the product described in this document.

The globe icon indicates a hyperlink that links directly to the Internet, where the latest updated information is available.
When no globe icon is present, the hyperlink links to specific elements and information within this document.

| | |
|---|---|
| *italics* | Folder, file and function names are printed in *italics*. |
| **bold** | **Bold** type is used for emphasis. |
| `mono` | A `monospaced` font type is used for hexadecimal numbers, listings, C function descriptions or wherever appropriate. Hexadecimal numbers are preceded by `"0x"`. |
| comment | Comments embedded into coding examples are shown in green text. |
| IRQ#<br>/IRQ | Signal names followed by a hashtag "#" or preceded by a forward slash "/" indicate that this signal is either active low or that it becomes active at a falling edge. |
| in/out | Signal directions in signal mnemonics tables generally refer to the corresponding board or component, "in" meaning "to the board or component", "out" meaning "from it the board or component". |

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Since July 1, 2006 all MEN standard products comply with RoHS legislation.

Since January 2005 the SMD and manual soldering processes at MEN have already been completely lead-free. Between June 2004 and June 30, 2006 MEN's selected component suppliers have changed delivery to RoHS-compliant parts. During this period any change and status was traceable through the MEN ERP system and the boards gradually became RoHS-compliant.

**WEEE Application**

The WEEE directive does not apply to fixed industrial plants and tools. The compliance is the responsibility of the company which puts the product on the market, as defined in the directive; components and sub-assemblies are not subject to product compliance.

In other words: Since MEN does not deliver ready-made products to end users, the WEEE directive is not applicable for MEN. Users are nevertheless recommended to properly recycle all electronic boards which have passed their life cycle.

Nevertheless, MEN is registered as a manufacturer in Germany. The registration number can be provided on request.



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# Contents

## Tables

## Figures

# 1 Getting Started

This chapter gives an overview of the board and some hints for first installation in a system.

## 1.1 Map of the Board

***Figure 1.*** *Map of the board – front view*

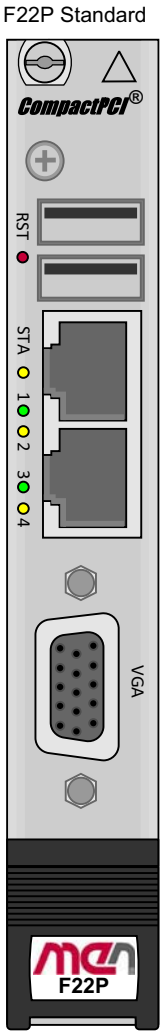
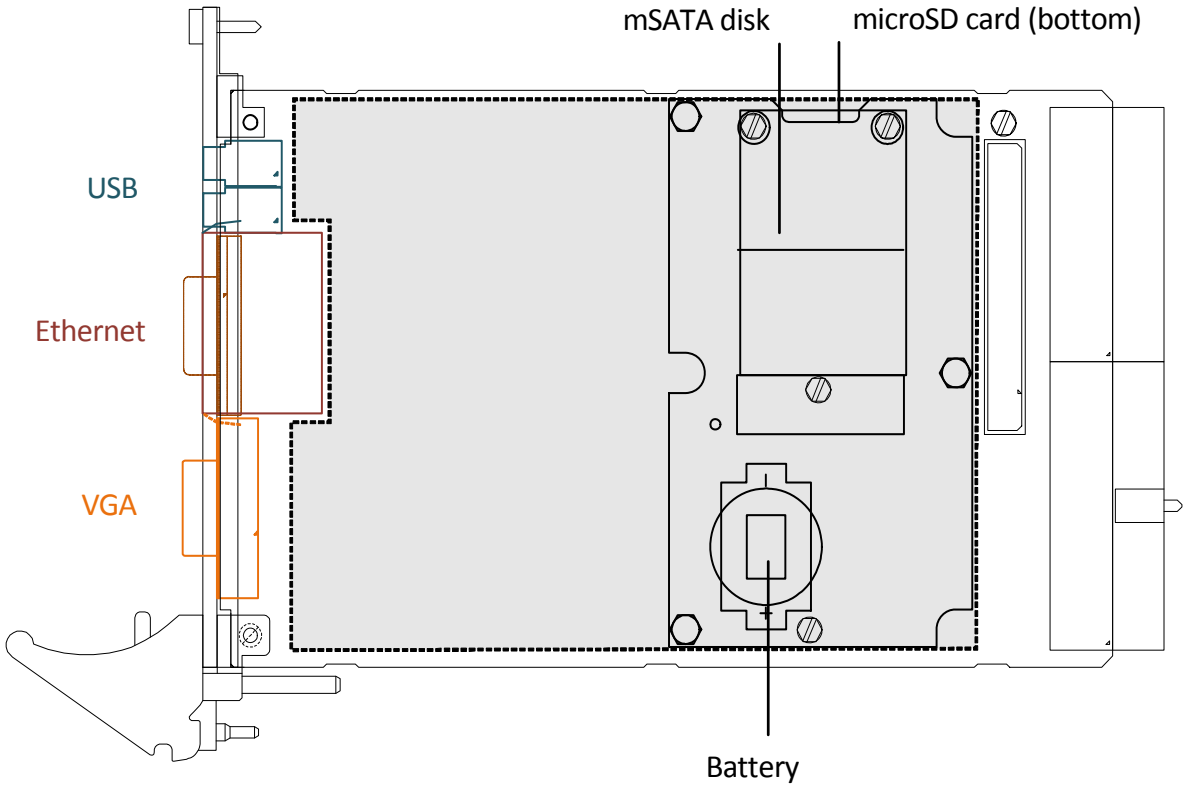


***Figure 2.*** *Map of the board – top view*



## 1.2 Configuring the Hardware

You should check your hardware requirements before installing the board in a system, since most modifications are difficult or even impossible to do when the board is mounted in a system.

The following check list gives an overview on what you might want to configure.

☑ microSD

The board is shipped without a microSD card. You should check your needs and install a suitable microSD card.

Refer to Chapter 2.9 Mass Storage on page 29 for more information on installation of the card.

☑ mSATA disk

The board is shipped without an mSATA disk. You should check your needs and install a suitable disk.

Refer to Chapter 2.9.3 mSATA Disk on page 31 for more information on installation of the card.

☑ Expansion by a side card

The board offers the option of adding one side card. Side cards come in standard 3U format and can be attached directly to F22P at the heat sink side. Every side card has dedicated functions, e.g. legacy COM interfaces, SATA hard disk or DVI front connectors.

The MEN sales staff will be glad to help you find the right extension and front panel solution. See also MEN's website for ordering information and standard products

Refer to Chapter 2.14 Side-Card Interface on page 38 for more details on side cards.

## 1.3 Integrating the Board into a System

You can use the following check list when installing the F22P in a system for the first time and with minimum configuration.

- ☑ Power-down the system.
- ☑ Remove all boards from the CompactPCI system.
- ☑ Insert the F22P into the system slot of your CompactPCI system, making sure that the CompactPCI connectors are properly aligned.

  Note: The system slot of every CompactPCI system is marked by a △ triangle on the backplane and/or at the front panel. It also has red guide rails.
- ☑ Connect a USB keyboard and mouse to the USB connectors at the front panel.
- ☑ Connect a CRT or flat-panel display to the VGA connector at the front panel.
- ☑ Power-up the system.
- ☑ You can start up the BIOS setup menu by hitting the <F2> key.
- ☑ Now you can make configurations in BIOS.

  For more information on the BIOS see Chapter 3 BIOS on page 55.
- ☑ Observe the installation instructions for the respective software.

## 1.4 Troubleshooting at Start-up

If you have any problems at start-up of the F22P, you can start the board with EFI default settings for troubleshooting.

Please refer to Chapter 3 BIOS on page 55.

## 1.5 Configuring BIOS

The F22P is equipped with an InsydeH2O UEFI framework. Normally you won't need to make any changes in the BIOS setup.

If you do, however, you'll find details on the BIOS in Chapter 3 BIOS on page 55.

## 1.6 Installing Operating System Software

The board supports Windows, Linux, VxWorks (on request) and QNX (on request)

By standard, no operating system is installed on the board. Please refer to the respective manufacturer's documentation on how to install operating system software!

You can find any software available on MEN's website.

### 1.6.1 Installing Windows XP or Windows 7 on USB Devices

The microSD card of the F22P is connected via USB. A standard Windows operating system (like Windows XP Professional or Windows 7 Ultimate) does not support direct installation on USB memory devices.

There are three possible solutions:

- Install the operating system on the mSATA disk of the F22P.
- Add a hard drive (SATA, mSATA) on a peripheral board or side card
- Switch to an Embedded Windows (like Windows Embedded Standard or Windows Embedded Standard 7). These Embedded Windows operating systems support being installed on and booted from a USB device.

Linux supports booting from a USB device without problems.

## 1.7 Installing Driver Software

For a detailed description on how to install driver software please refer to the respective documentation.

You can find any driver software and documentation available for download on MEN's website.

# 2 Functional Description

The following describes the individual functions of the board and their configuration on the board. There is no detailed description of the individual controller chips and the CPU. They can be obtained from the data sheets or data books of the semiconductor manufacturer concerned..

Also see Chapter 5.1 Literature and Web Resources on page 79.

## 2.1 Power Supply

There are only two possible ways to power the F22P:

- +5V, +3.3V **and** +12V via CompactPCI connector J1
- +5V **only** via CompactPCI connector J1

To supply the board with 3.3V and 5V is not allowed and may cause serious damage. If +3.3V are supplied via CompactPCI connector J1, the +12V supply always has to be present.

If the +12V are not present, the board automatically generates +3.3V and also feeds them to the backplane, which would cause a conflict with the external +3.3V supply.

## 2.2 Board Supervision

The F22P provides an intelligent board management controller (BMC) with the following main features:

- Board power sequencing control
- Voltage supervision
- System watchdog
- Software reset functionality
- Error state logging
- Power mode settings
- SMBus communication with main CPU

The watchdog device monitors the board on operating system level. If enabled, the watchdog must be triggered by application software. If the trigger is overdue, the watchdog initiates a board reset and this way can put the system back into operation when the software hangs.

The watchdog uses a configurable time interval or is disabled. Settings are made through BIOS or via an MEN software driver.

In addition, the F22P uses a temperature device to measure the local board temperature.

MEN provides dedicated software drivers for the board controller and the temperature device. For a detailed description of the functionality of the driver software please refer to the drivers' documentation.

You can find any driver software and documentation available for download on MEN's website.

## 2.3 Intel Active Management Technology (AMT)

F22P boards equipped with an Intel Core i7 or i5 processor support Intel Active Management Technology (AMT 8.0). Intel AMT is powered by a separate hardware engine in Intel chipsets which enables e.g. out-of-band (OOB) diagnostics, remote control, IDE-Redirect, Serial-over-LAN (SOL), agent presence checking and network traffic filtering.

AMT is supported on the lower front Ethernet interface (ETH2) of the F22P.

For information on how to enable the AMT BIOS extension see Chapter 3 BIOS.

MEN provides an application note on how to switch on the AMT functionality and log onto the CPU board via VNC afterwards. See MEN's website.

If the supercapacitor and/or the battery is empty, the F22P loses its complete AMT settings due to Intel's security standards.

As an option, a BIOS setting can be implemented which makes it possible to switch the AMT interface to the backplane via the Ethernet rear I/O card. In this case, there is only one Ethernet interface (ETH1) available at the front panel.

Please contact MEN's sales team for further information.

## 2.4 Trusted Platform Module

A trusted platform module to protect the content of the SATA storage devices is available on the F22P. The TPM module is compliant to the TPM v1.2 specification.

## 2.5 Reset Behavior and Power States

The F22P can be reset using the reset button on the front panel or the *PBRST#* signal on the backplane. It supports the S5, S4, S3, S0 and Mx power states. All voltages which are not required are deactivated while the board is into a lower power state.

See also Chapter 2.17 Reset Button and Status LED on page 53.

## 2.6 Real-Time Clock

The board includes a real-time clock connected to the chipset. For data retention during power off the RTC is backed up by a supercapacitor. The supercapacitor gives an autonomy of approx. 14 hours when fully loaded. Under normal conditions, replacement should be superfluous during lifetime of the board. The RTC can generate interrupt requests to the chipset.

The RTC has an accuracy of approximately 1.7 seconds/day (11 minutes/year) at 25°C.

For retention of time/date data after a power off of more than 8-10 hours the RTC is also backed by a battery.

For ordering options please see MEN's website.

## 2.7 Processor Core

The F22P can be equipped with different types of Intel i7, i5, i3 or Celeron processors. The following table gives a performance overview:

***Table 1.*** *Processor core options on F22P*

| Processor Type | Core Frequency | Cores/ Threads | Power Consumption | Cache | AMT Support |
|---|---|---|---|---|---|
| Core i7-3615QE | 2.3 GHz | 4/8 | 45 W | 6 MB | yes |
| Core i7-3612QE | 2.1 GHz | 4/8 | 35 W | 6 MB | yes |
| Core i7-3555LE | 2.5 GHz | 2/4 | 25 W | 4 MB | yes |
| Core i7-3517UE | 1.7 GHz | 2/4 | 17 W | 4 MB | yes |
| Core i5-3610ME | 2.7 GHz | 2/4 | 35 W | 3 MB | yes |
| Core i3-3120ME | 2.4 GHz | 2/4 | 35 W | 3 MB | no |
| Core i3-3217UE | 1.6 GHz | 2/4 | 17 W | 3 MB | no |
| Celeron 1020E | 2.2 GHz | 2/2 | 35 W | 2 MB | no |
| Celeron 1047UE | 1.4 GHz | 2/2 | 17 W | 2 MB | no |
| Celeron 927UE[1] | 1.5 GHz | 1/1 | 17 W | 1 MB | no |

[1] without PCI Express® on side card

### 2.7.1 Thermal Considerations

A suitable heat sink is provided to meet thermal requirements. For special requirements a larger heat sink is also available on request.

Please contact MEN sales for more information.

Please note that if you use any other heat sink than that supplied by MEN, or no heat sink at all, warranty on functionality and reliability of the F22P may cease. If you have any questions or problems regarding thermal behavior, please contact MEN.

## 2.8 Memory

The standard board versions provide a memory configuration suitable for many applications. However, memory on the F22P can also be configured for your needs.

For standard memory sizes and ordering options please see MEN's website.

### 2.8.1 DRAM System Memory

The board provides up to 16 GB onboard, soldered DDR3 (double data rate) SDRAM. The memory bus is 2x72 bits wide (dual channel) and operates with up to 1066 MHz.

### 2.8.2 Boot Flash

The F22P has an 64-Mbit SPI Serial Flash implemented as onboard Flash for BIOS data.

## 2.9 Mass Storage

The F22P offers six SATA lines on the J2 rear I/O connector and the side card connector.

For more information see Chapter 2.9.1 Serial ATA (SATA).

The board offers the possibility to connect an mSATA disk on a small adapter card in the heat sink area which is assembled by standard.

For more information see Chapter 2.9.3 mSATA Disk.

In addition, the board offers the possibility to connect an microSD card on a small adapter card in the heat sink area which is assembled by standard.

For more information see Chapter 2.9.2 microSD Card.

### 2.9.1 Serial ATA (SATA)

The serial ATA (SATA) interface is controlled by the platform controller hub and provides six SATA channels.

In compliance with the CompactPCI PlusIO standard PICMG 2.30 four of these interfaces are led to the J2 rear I/O connector.

One SATA channel is led to the side-card connector. The device can be connected through the use of a side card. The sixth channel is used for the mSATA disk.

Four interfaces are compliant to SATA revision 2.x (3.0 Gb/s). Two of the interfaces on the J2 rear I/O connector are compliant to SATA revision 3.x (6.0 Gb/s). The interfaces can be run in AHCI and RAID mode. RAID 0, 1, 5 and 10 are supported.

See Chapter 2.14 Side-Card Interface on page 38 for further details on the side-card interface, and Chapter 2.16.1 CompactPCI PlusIO Rear I/O on page 48 for information on the rear I/O.

### 2.9.2 microSD Card

The F22P provides an onboard microSD card slot on the bottom side of the mSATA adapter card in the heat sink area. The slot is ready-to-use. The F22P is shipped without a microSD card installed.

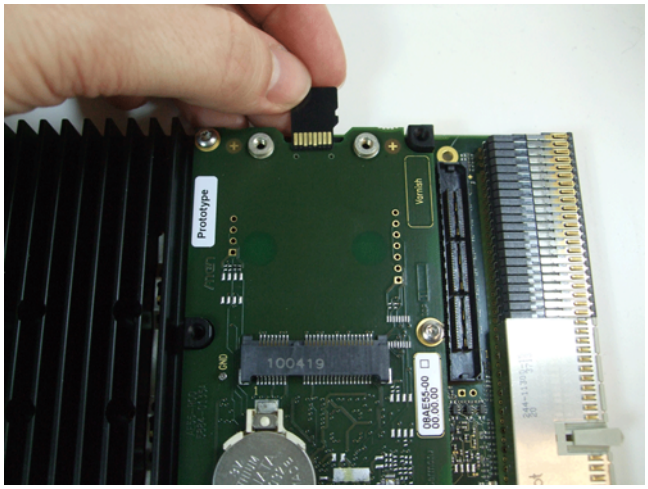
Please see MEN's website for ordering options.

#### 2.9.2.1 Inserting and Extracting a microSD Card

The microSD card has to be installed before the mSATA disk as it is difficult to access it afterwards.

To install a microSD card, please stick to the following procedure.

- ☑ Power down your system and remove the F22P from the system.
- ☑ Put the board on a flat surface.
- ☑ Insert the microSD card into the slot with the contacts at the top.




- ☑ Make sure that it clicks into place properly.
- ☑ For extracting the card push it down and pull it out.

### 2.9.3 mSATA Disk

The mSATA disk is controlled via a SATA channel from the chipset. The F22P is shipped without an mSATA disk installed.

Please see MEN's website for ordering options.

#### 2.9.3.1 Installing an mSATA Disk

To install an mSATA disk, please stick to the following procedure.

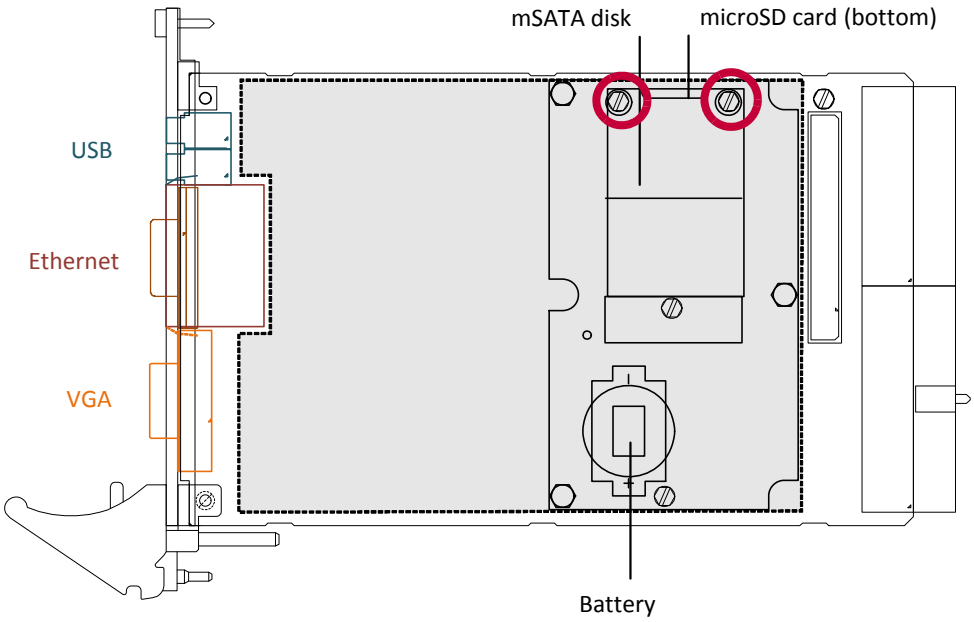
☑ Power down your system and remove the F22P from the system.

☑ Put the board on a flat surface.

☑ Insert the mSATA disk carefully in a 30° angle.

☑ Make sure that all the contacts are aligned properly and the card is firmly connected with the card connector.

☑ Fix the card using two M2.5 x4 screws and two spacers (highlighted in red).



## 2.10 Graphics

The graphics subsystem is part of the Intel QM67 Platform Controller Hub and supports VGA as well as different digital display interfaces (HDMI, DisplayPort and SDVO).

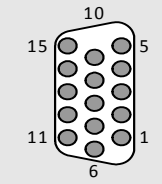
### 2.10.1 VGA Front Connection

You can connect a VGA monitor directly at the F22P's front panel. The pinout of the 15-pin HD-Sub connector is standard VGA.

Connector types:

- 15-pin HD-Sub receptacle according to DIN41652/MIL-C-24308, with thread bolt UNC 4-40
- Mating connector:
  15-pin HD-Sub plug according to DIN41652/MIL-C-24308, available for ribbon cable (insulation piercing connection), hand-soldering connection or crimp connection

***Table 2.*** *Pin assignment of 15-pin HD-Sub VGA receptacle connector*




| | | | | | |
|---|---|---|---|---|---|
| 15 | SCL | 10 | GND | 5 | GND |
| 14 | VSYNC | 9 | - | 4 | - |
| 13 | HSYNC | 8 | GND | 3 | B |
| 12 | SDA | 7 | GND | 2 | G |
| 11 | - | 6 | GND | 1 | R |

***Table 3.*** *Signal mnemonics of 15-pin HD-Sub VGA connector*

| Signal | Direction | Function |
|---|---|---|
| GND | - | Ground |
| HSYNC | out | Horizontal synchronization |
| R, G, B | out | Analog monitor interface (red, green, blue) |
| SCL | out | Monitor I²C interface |
| SDA | in/out | |
| VSYNC | out | Vertical synchronization |

### 2.10.2 VGA Rear Connection

For conduction-cooled versions of the F22P, there is the possibility to lead a display data channel to the backplane via the J1 CompactPCI connector.

### 2.10.3 Connection via Digital Display Interface

The F22P provides two digital display interfaces on the side-card connector. One supports SDVO, DisplayPort and HDMI, the other only DisplayPort and HDMI. Embedded audio is also supported on DisplayPort and HDMI.

One DVI interface can be implemented using the SDVO interface on an MEN side card. .

See MEN's website for available side cards.

For possibilities to implement DisplayPort or HDMI using a side card please contact MEN's sales team.

Also see Chapter 2.14 Side-Card Interface on page 38 for further details on the side-card interface.

## 2.11 USB Interfaces

The F22P provides eleven USB 2.0 ports controlled by the chipset. Two USB interfaces are routed to standard front-panel connectors, four are led to the side-card connector, and another four can be accessed on the CompactPCI J2 rear I/O connector (compliant to the CompactPCI PlusIO standard). The remaining interface is used for connection of the microSD card. The USB interfaces support UHCI.

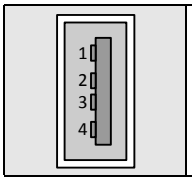
### 2.11.1 Front-Panel Connection

Two USB interfaces are accessible at the front panel.

Connector types:

- 4-pin USB Series A receptacle according to Universal Serial Bus Specification Revision 1.0
- Mating connector:
  4-pin USB Series A plug according to Universal Serial Bus Specification Revision 1.0

***Table 4.*** *Pin assignment of USB front-panel connectors*




| | |
|---|---|
| 1 | +5V |
| 2 | USB_D- |
| 3 | USB_D+ |
| 4 | GND |

***Table 5.*** *Signal mnemonics of USB front-panel connectors*

| Signal | Direction | Function |
|---|---|---|
| +5V | out | +5 V power supply |
| GND | - | Digital ground |
| USB_D+, USB_D- | in/out | USB lines, differential pair |

### 2.11.2 Side-Card Connection

Four USB interfaces are accessible via a side card.

Also see Chapter 2.14 Side-Card Interface on page 38 for further details on the side-card interface.

See MEN's website for available side cards and board versions.

### 2.11.3 Rear I/O Connection (CompactPCI PlusIO)

Four USB interfaces are accessible via rear I/O in compliance to the CompactPCI PlusIO standard PICMG 2.30.

See Chapter 2.16.1 CompactPCI PlusIO Rear I/O on page 48 for detailled information on the J2 rear I/O pin assignments.

## 2.12 Ethernet Interfaces

The F22P has three Ethernet interfaces connected to the processor and the PCH via three x1 PCI Express (PCIe) links. They are controlled by two Intel 82574L Ethernet controllers and one Intel 82579LM Ethernet PHY. They support 10 Mbits/s up to 1000 Mbits/s as well as full-duplex operation and autonegotiation. The lower front interface supports AMT.

The unique MAC address is set at the factory and should not be changed. Any attempt to change this address may create node or bus contention and thereby render the board inoperable. The naming of the interfaces may differ depending on the operating system.

### 2.12.1 Front-Panel Connection

Two standard RJ45 connectors are available at the front panel. There are two status LEDs for each channel at the front panel.

The pin assignment corresponds to the Ethernet specification IEEE802.3.

***Table 6.*** *Signal mnemonics of Ethernet 10/100/1000Base-T connectors*

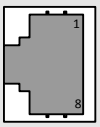
| Signal | Direction | Function |
|---|---|---|
| BI_Dx+/- | in/out | Differential pairs of data lines for 1000Base-T |
| RX+/- | in | Differential pair of receive data lines for 10/100Base-T |
| TX+/- | out | Differential pair of transmit data lines for 10/100Base-T |

#### 2.12.1.1 Connection via RJ45 Connectors

Connector types:

- Modular 8/8-pin mounting jack according to FCC68
- Mating connector:
  Modular 8/8-pin plug according to FCC68

***Table 7.*** *Pin assignment and status LEDs of 8-pin RJ45 Ethernet 10/100/1000Base-T connectors (LAN1/LAN2)*

| | | | | |
|---|---|---|---|---|
| On: Link up<br>Off: Link down | L |  | 1 | BI_DA+ |
| | | | 2 | BI_DA- |
| | | | 3 | BI_DB+ |
| | | | 4 | BI_DC+ |
| On: Transmit or receive activity<br>Off: No transmit or receive activity<br>Blinking: Transmit or receive activity | A | | 5 | BI_DC- |
| | | | 6 | BI_DB- |
| | | | 7 | BI_DD+ |
| | | | 8 | BI_DD- |

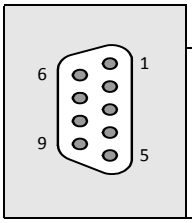
#### 2.12.1.2 Connection via 9-pin D-Sub Connector (optional)

A D-Sub connector can be implemented as an option. In this case, only 10Base-T and 100Base-TX are supported, no Gigabit Ethernet connection. The two interfaces are routed to one D-Sub connector.

Connector types:

- 9-pin D-Sub plug according to DIN41652/MIL-C-24308, with thread bolt UNC 4-40
- Mating connector:
  9-pin D-Sub receptacle according to DIN41652/MIL-C-24308, available for ribbon cable (insulation piercing connection), hand-soldering connection or crimp connection

***Table 8.*** *Pin assignment of 9-pin D-Sub 10Base-T/100Base-TX plug connector (LAN1/LAN2)*




| | | | |
|---|---|---|---|
| | | 1 | LAN2_TX+ |
| 6 | LAN2_TX- | 2 | LAN1_TX+ |
| 7 | LAN1_TX- | 3 | - |
| 8 | LAN1_RX- | 4 | LAN1_RX+ |
| 9 | LAN2_RX- | 5 | LAN2_RX+ |

### 2.12.2 Rear I/O Connection

The third Ethernet interface is controlled via a PCI Express x1 link from the processor and available at the J2 rear I/O connector in compliance with CompactPCI PlusIO standard PICMG 2.30.

As an option, one of the front Ethernet interfaces can be led to the J2 connector. A special board version is required for this. On this board version the lower front Ethernet interface with AMT functionality cannot be used.

Please contact MEN's sales staff for further information.

For the J2 rear I/O pin assignments see Chapter 2.16.1 CompactPCI PlusIO Rear I/O on page 48.

## 2.13 High Definition (HD) Audio Interface

The F22P provides an HD audio interface accessible via a side card. Embedded audio on DisplayPort and HDMI is supported.

See Chapter 2.14 Side-Card Interface on page 38 for further details on the side-card interface.

See MEN's website for available side cards.

See Chapter 5.1 Literature and Web Resources on page 79 for literature on HD audio.

## 2.14 Side-Card Interface

MEN offers a number of side cards for F22P, featuring different I/O functionality. The side cards are all standard 3U Eurocards in 4 HP (single) width. Access to I/O connectors is given directly from the front panel.

The side-card connector is located at the top side of the board, so that one side card can be attached to the right side of the F22P. As an option, the F22P can also be supplied with the side-card connector at the bottom side, so that the side card may be attached to the left side of the CPU.

The side-card connector on F22P supports the following interfaces:

- One SATA channel (switchable to port A or B via BIOS)
- Four USB interfaces
- Three PCI Express x1 links
- HD audio interface
- One digital video output supporting SDVO, DisplayPort and HDMI (Port B)
- One digital video output supporting DisplayPort and HDMI (Port C)

See MEN's website for available side cards and board versions.

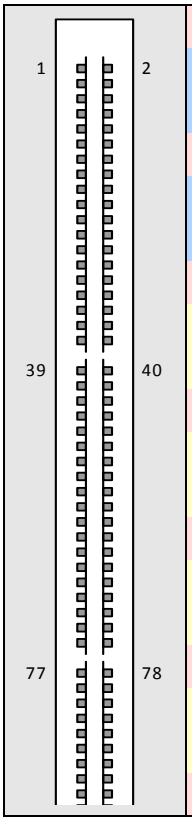
Neither the +3.3V nor the +5V pins of the expansion interface connector are protected against a short-circuit situation! This connector therefore should be used exclusively for attachment of a side card.

### 2.14.1 Connection

Connector types:

- 114-pin matched impedance receptacle connector, MICTOR 0.64 mm grid
- Mating connector:
  114-pin matched impedance plug connector, MICTOR 0.64 mm grid

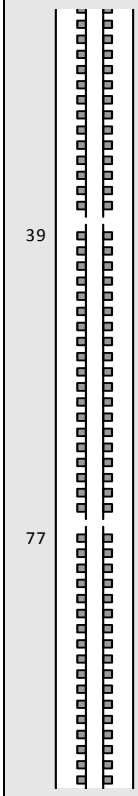
***Table 9.*** *Pin assignment of 114-pin side-card connector, pins 1..38*




| | | | | |
|---|---|---|---|---|
| 1 | GND | | 2 | GND |
| 3 | SATA_A_TX+ | | 4 | SATA_B_TX+ |
| 5 | SATA_A_TX- | | 6 | SATA_B_TX- |
| 7 | GND | | 8 | GND |
| 9 | SATA_A_RX+ | | 10 | SATA_B_RX+ |
| 11 | SATA_A_RX- | | 12 | SATA_B_RX- |
| 13 | GND | | 14 | GND |
| 15 | PCIE1_TX+ | | 16 | PCIE3_TX+ |
| 17 | PCIE1_TX- | | 18 | PCIE3_TX- |
| 19 | GND | GND | 20 | GND |
| 21 | PCIE1_RX+ | | 22 | PCIE3_RX+ |
| 23 | PCIE1_RX- | | 24 | PCIE3_RX- |
| 25 | GND | | 26 | GND |
| 27 | PCIE0_TX+ | | 28 | PCIE2_TX+ |
| 29 | PCIE0_TX- | | 30 | PCIE2_TX- |
| 31 | GND | | 32 | GND |
| 33 | PCIE0_RX+ | | 34 | PCIE2_RX+ |
| 35 | PCIE0_RX- | | 36 | PCIE2_RX- |
| 37 | GND | | 38 | GND |

Note: There is one SATA port on the side-card connector which can be switched to Port A or Port B via the BIOS. PCI Express port 3 can be implemented on a special board version instead of port 1.

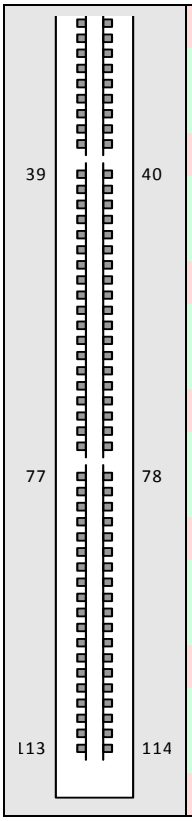
***Table 10.*** *Pin assignment of 114-pin side-card connector, pins 39..76*




| | | | | | |
|---|---|---|---|---|---|
| | | 39 | +3.3V | | 40 | +3.3V |
| | | 41 | USB_1_2_OC# | | 42 | HDA_SYNC |
| | | 43 | USB_3_4_OC# | | 44 | HDA_BIT_CLK |
| | | 45 | GND | | 46 | HDA_RST# |
| | | 47 | USB_D3- | | 48 | HDA_SDOUT |
| | | 49 | USB_D3+ | | 50 | HDA_SDIN |
| 39 | 40 | 51 | GND | | 52 | GND |
| | | 53 | USB_D1- | | 54 | PCIE_WAKE# |
| | | 55 | USB_D1+ | | 56 | PLT_RST# |
| | | 57 | GND | | 58 | - |
| | | 59 | USB_D5- | +5V | 60 | SMB_CLK |
| | | 61 | USB_D5+ | | 62 | SMB_DATA |
| | | 63 | GND | | 64 | GND |
| 77 | 78 | 65 | USB_D4- | | 66 | DPB_OB_AUX_p/ SDVO_CTRLCLK |
| | | 67 | USB_D4+ | | 68 | DPB_OB_AUX_n/ SDVO_CTRLDATA |
| | | 69 | GND | | 70 | GND |
| | | 71 | PCIE_CLK_A_REF+ | | 72 | PCIE_CLK_B_REF+ |
| | | 73 | PCIE_CLK_A_REF- | | 74 | PCIE_CLK_B_REF- |
| | | 75 | GND | | 76 | GND |

Note: The signals marked in gray are multiplexed.

***Table 11.*** *Pin assignment of 114-pin side-card connector, pins 77..114*




| | | | | |
|---|---|---|---|---|
| 77 | GND | | 78 | GND |
| 79 | SDVO_TVCLKIN- | | 80 | SDVO_FLDSTALL- |
| 81 | SDVO_TVCLKIN+ | | 82 | SDVO_FLDSTALL+ |
| 83 | GND | | 84 | GND |
| 85 | DDPB_[2]_n | | 86 | DDPC_[2]_n |
| 87 | DDPB_[2]_p | | 88 | DDPC_[2]_p |
| 89 | GND | | 90 | GND |
| 91 | DDPB_[1]_n | | 92 | DDPC_[1]_n |
| 93 | DDPB_[1]_p | | 94 | DDPC_[1]_p |
| 95 | GND | GND | 96 | GND |
| 97 | DDPB_[0]_n | | 98 | DDPC_[0]_n |
| 99 | DDPB_[0]_p | | 100 | DDPC_[0]_p |
| 101 | GND | | 102 | GND |
| 103 | DDPB_[3]_n | | 104 | DDPC_[3]_n |
| 105 | DDPB_[3]_p | | 106 | DDPC_[3]_p |
| 107 | GND | | 108 | GND |
| 109 | SDVO_INT- | | 110 | DDP_CTRDATA |
| 111 | SDVO_INT+ | | 112 | DDP_CTRLCLK |
| 113 | GND | | 114 | DDPC_HPD |

***Table 12.*** *Signal mnemonics of 114-pin side-card connector*

| | Signal | Direction | Function |
|---|---|---|---|
| **Power** | +3.3V | out | +3.3 V power supply |
| | +5V | out | +5 V power supply |
| | GND | - | Digital ground of respective interface |
| **SATA (Port A or B depending on BIOS setting)** | SATA_A_RX+, SATA_A_RX- | in | Differential pair of SATA receive lines, port A |
| | SATA_A_TX+, SATA_A_TX- | out | Differential pair of SATA transmit lines, port A |
| | SATA_B_RX+, SATA_B_RX- | in | Differential pair of SATA receive lines, port B |
| | SATA_B_TX+, SATA_B_TX- | out | Differential pair of SATA transmit lines, port B |
| **PCI Express** | PCIE_CLK_A_REF+, PCIE_CLK_A_REF- | out | Reference clock A 100 MHz |
| | PCIE_CLK_B_REF+, PCIE_CLK_B_REF- | out | Reference clock B 100 MHz |
| | PCIE0_RX+, PCIE0_RX- | in | Differential pair of PCIe receive lines, port 0 |
| | PCIE0_TX+, PCIE0_TX- | out | Differential pair of PCIe transmit lines, port 0 |
| | PCIE1_RX+, PCIE1_RX- | in | Differential pair of PCIe receive lines, port 1 |
| | PCIE1_TX+, PCIE1_TX- | out | Differential pair of PCIe transmit lines, port 1 |
| | PCIE2_RX+, PCIE2_RX- | in | Differential pair of PCIe receive lines, port 2 |
| | PCIE2_TX+, PCIE2_TX- | out | Differential pair of PCIe transmit lines, port 3 |
| | PCIE3_RX+, PCIE3_RX- | in | Differential pair of PCIe receive lines, port 3 (optional, can be implemented on a special board version instead of port 1) |
| | PCIE3_TX+, PCIE3_TX- | out | Differential pair of PCIe transmit lines, port 3 |
| | PCIE_WAKE# | in | Wake signal from PCIe device to wake F22P from sleep state |
| **USB** | USB_D[1]+, USB_D[1]- | in/out | Differential pair of USB lines, port 2 |
| | USB_D[2]+, USB_D[2]- | in/out | Differential pair of USB lines, port 3 |
| | USB_D[3]+, USB_D[3]- | in/out | Differential pair of USB lines, port 4 |
| | USB_D[4]+, USB_D[4]- | in/out | Differential pair of USB lines, port 5 |
| | USB_OC12# | in | USB overcurrent, ports 1and 2 |
| | USB_OC34# | in | USB overcurrent, ports 3 and 4 |

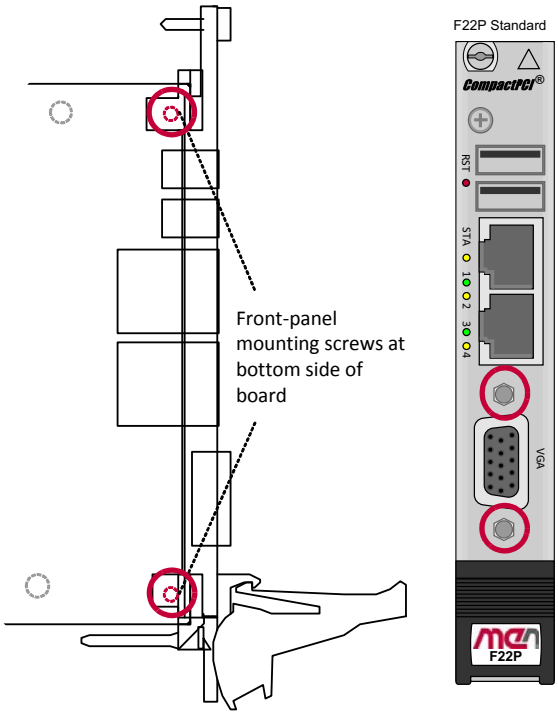
| | Signal | Direction | Function |
|---|---|---|---|
| **HD Audio** | HDA_BIT_CLK | in/out | HD Audio serial data clock |
| | HDA_RST# | out | HD Audio reset |
| | HDA_SDIN | in | HD Audio serial data in |
| | HDA_SDOUT | out | HD Audio serial data out |
| | HDA_SYNC | out | HD Audio synchronization |
| **Digital Display Interface (DDP)** | DDPB_[x]_n, DDPB_[x]_p, | out | Digital display interface B data, differential pair |
| | DDPC_[x]_n, DDPC_[x]_p, | out | Digital display interface C data, differential pair |
| | DDP_CTRDATA | in/out | Digital display interface control data |
| | DDP_CTRLCLK | in/out | Digital display interface control clock |
| | DDPC_HPD | in | Digital display interface hot plug detect |
| | DPB_OB_AUX_n, DPB_OB_AUX_p (shared with SDVOCTRL_CLK and SDVOCTRL_DATA | in/out | Digital display interface auxiliary lines, needed when interface B is used as DisplayPort or HDMI |
| | SDVOB_INT+, SDVOB_INT- | in | Serial digital video input interrupt, differential pair |
| | SDVO_FLDSTALL+, SDVO_FLDSTALL- | in | Serial digital video field stall, differential pair |
| | SDVO_TVCLKIN+, SDVO_TVCLKIN- | in | Serial digital video TVOUT synchronization clock, differential pair |
| | SDVOCTRL_CLK (shared with DPB_OB_AUX_p) | in/out | I2C based control signal (clock) for SDVO device, needed when interface B is used as SDVO |
| | SDVOCTRL_DATA (shared with DPB_OB_AUX_n) | in/out | I2C based control signal (data) for SDVO device, needed when interface B is used as SDVO |
| **Other** | PLT_RST# | out | Platform reset (global reset) |
| | SMB_CLK | out | System Management Bus clock |
| | SMB_DATA | in/out | System Management Bus data |

### 2.14.2 Installing a Side Card

Perform the following steps to install a side card:

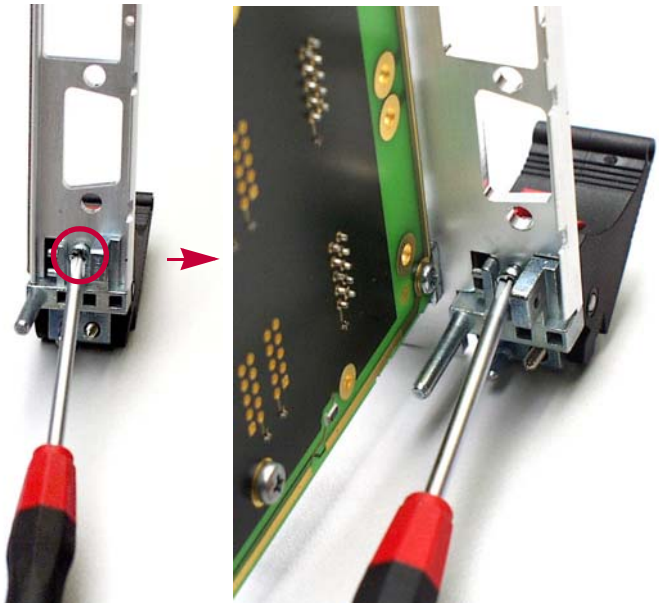
☑ Power-down your system and remove the F22P from the system.

☑ Remove the front panel: Loosen and remove the screws highlighted in red.

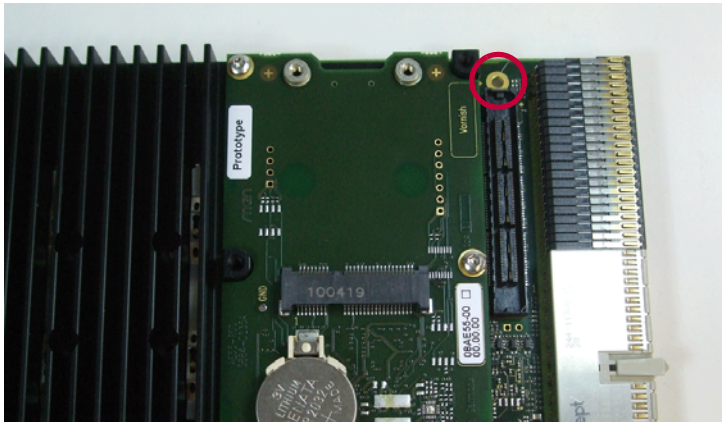



☑ Remove the front-panel ejector from the F22P front panel: Loosen the ejector screw at the back of the front panel.

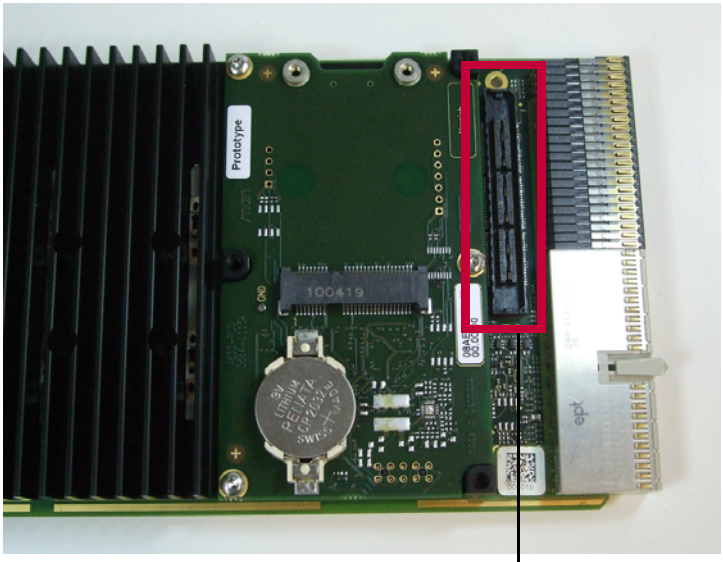
☑ Install the ejector on the side card's front panel.

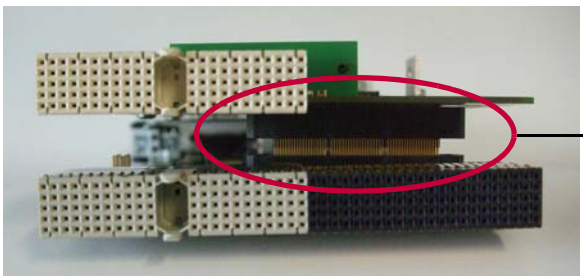


☑ Install the side card standoff supplied with the side card in the mounting hole indicated in red in the following picture.
Note that two different standoffs are supplied with the side card. For the F22P the longer standoff (M2x18 I/I) is required.

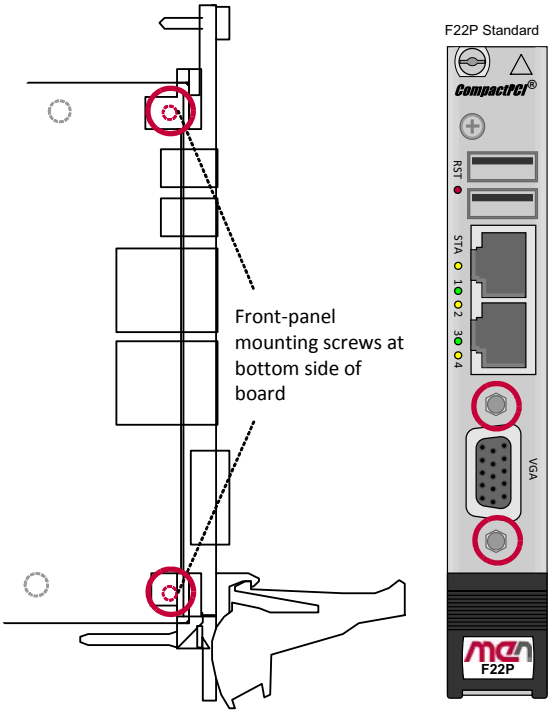



☑ Each side card comes with a dedicated one-piece, two-slot front panel. Align the F22P's front panel connectors with the side card's front panel, and align the board-to-board connector of the side card with the side-card connector of F22P. Press the board-to-board connectors together.

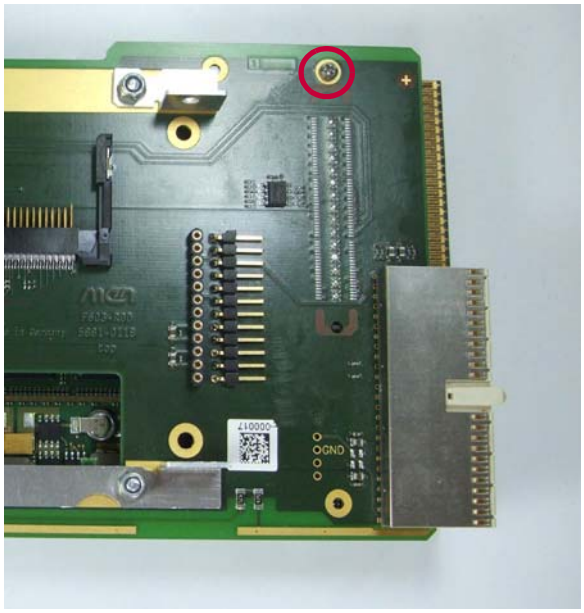


☑ Fasten the front panel: Install the screws removed before as highlighted in red.




☑ Fasten the side-card standoff using the spring and screw provided with the side card at the top of the side card.



☑ Reinsert the board into your system.

## 2.15 PCI Express

### 2.15.1 General

PCI Express (PCIe) succeeds PCI and AGP and offers higher data transfer rates.

As opposed to the PCI bus, PCIe is no parallel bus but a serial point-to-point connection. Data is transferred using so-called lanes, with each lane consisting of a line pair for transmission and a second pair for reception. Individual components are connected using switches.

At the electrical level, each lane consists of two unidirectional LVDS (Low Voltage Differential Signaling) pairs. Transmit and receive are separate differential pairs, for a total of 4 data wires per lane.

PCIe supports full-duplex operation and uses a clock rate of 1.25 GHz. This results in a data rate of max. 250 MB/s per lane in each direction. (The standard PCI bus with 32 bits/33 MHz only allows a maximum of 133 MB/s.)

If you use only one lane, you speak of a PCIe x1 link. You can couple several lanes to increase the data rate, e.g. x2 with 2 lanes up to a x32 link using 32 lanes.

In addition, PCIe supports hot plug, for instance to exchange defect expansion boards during operation.

In terms of software, most operating systems can handle PCI Express boards just as well as the old PCI.

### 2.15.2 Implementation on F22P

On F22P the three Gigabit Ethernet channels are permanently connected via PCIe x1 links. Another three x1 links are available for use over a side card. This means that the side card implementation determines the usage of these three links.

Four PCIe x1 links are led to the J2 rear I/O connector in compliance with the CompactPCI PlusIO standard PICMG 2.30. The interfaces on the J2 connector and the side-card connector support the PCI Express specification 2.x with a data transfer rate of 5 Gbits/s per lane.

## 2.16 CompactPCI Interface

The F22P is a 3U CompactPCI system slot board. It implements a 32-bit PCI interface to the CompactPCI backplane which uses a +3.3 V signaling voltage. It also tolerates +5 V.

The CompactPCI bus connects to the processor via a PCI-Express-to-PCI-Bridge. The board supports seven external PCI bus devices.

In combination with a specific side card the F22P can also perform system-slot functionality in a CompactPCI Express system.

### 2.16.1 CompactPCI PlusIO Rear I/O

The F22P is also compliant to the CompactPCI PlusIO standard PICMG 2.30. This means that it offers a fixed pin assignment of one Gigabit Ethernet, 4 SATA, 4 PCI Express and 4 USB interfaces at the J2 connector. A second Gigabit Ethernet interface can be implemented by switching one front interface to the rear.

As a result, the pin assignment of the F22P rear I/O connector J2 is not compliant anymore to the rear I/O of the F14, F15, F17 and F18.

MEN offers a rear I/O transition module on which all interfaces from the J2 connector can be accessed, the CT12.

Note: The F22P supports one Gigabit Ethernet interface at the rear whereas the PICMG 2.30 CompactPCI PlusIO standard supports up to two.

See MEN's website for further information.

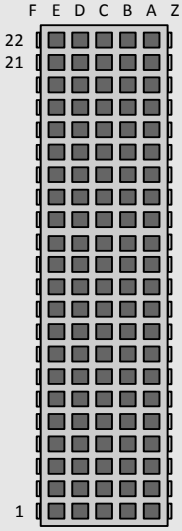
### 2.16.2 CompactPCI Connector J1

The pin assignment of connector J1 as defined in the CompactPCI specification will not be repeated here. The voltage supply for the battery can optionally be made available on the A4 pin on the conduction-cooled board version.

### 2.16.3 CompactPCI Connector J2

The table below shows the fixed pinout of the J2 connector as defined in the PICMG 2.30 CompactPCI PlusIO standard.

***Table 13.*** *Pin assignment of CompactPCI connector J2*




| | F | E | D | C | B | A | Z |
|---|---|---|---|---|---|---|---|
| 22 | GND | GA0 | GA1 | GA2 | GA3 | GA4 | GND |
| 21 | GND | 1_ETH_B+ | 1_ETH_D+ | 2_ETH_B+ | GND | CLK6 | GND |
| 20 | GND | 1_ETH_B- | 1_ETH_D- | 2_ETH_B- | GND | CLK5 | GND |
| 19 | GND | 1_ETH_A+ | 1_ETH_C+ | 2_ETH_A+ | GND | GND | GND |
| 18 | GND | 1_ETH_A- | 1_ETH_C- | 2_ETH_A- | 2_ETH_C+ | 2_ETH_D+ | GND |
| 17 | GND | GNT6# | REQ6# | PBRST# | 2_ETH_C- | 2_ETH_D- | GND |
| 16 | GND | CRT_R_D-DC_CLK | GND | DEG# | 2_PE_CLK+ | 4_PE_CLK- | GND |
| 15 | GND | GNT5# | REQ5# | FAIL# | 2_PE_CLK- | 4_PE_CLK+ | GND |
| 14 | GND | PWRBTN# | SATA_SCL | 4_PE_CLKE# | 1_PE_CLK+ | 3_PE_CLK- | GND |
| 13 | GND | SATA_SL | SATA_SDO | 3_PE_CLKE# | 1_PE_CLK- | 3_PE_CLK+ | GND |
| 12 | GND | 4_SATA_Rx+ | SATA_SDI | 2_PE_CLKE# | 1_PE_CLKE# | 4_PE_Rx00+ | GND |
| 11 | GND | 4_SATA_Rx- | 4_SATA_Tx+ | 4_USB2+ | 4_PE_Tx00+ | 4_PE_Rx00- | GND |
| 10 | GND | 3_SATA_Rx+ | 4_SATA_Tx- | 4_USB2- | 4_PE_Tx00- | 3_PE_Rx00+ | GND |
| 9 | GND | 3_SATA_Rx- | 3_SATA_Tx+ | 3_USB2+ | 3_PE_Tx00+ | 3_PE_Rx00- | GND |
| 8 | GND | 2_SATA_Rx+ | 3_SATA_Tx- | 3_USB2- | 3_PE_Tx00- | 2_PE_Rx00+ | GND |
| 7 | GND | 2_SATA_Rx- | 2_SATA_Tx+ | 2_USB2+ | 2_PE_Tx00+ | 2_PE_Rx00- | GND |
| 6 | GND | 1_SATA_Rx+ | 2_SATA_Tx- | 2_USB2- | 2_PE_Tx00- | 1_PE_Rx00+ | GND |
| 5 | GND | 1_SATA_Rx- | 1_SATA_Tx+ | 1_USB2+ | 1_PE_Tx00+ | 1_PE_Rx00- | GND |
| 4 | GND | CRT_R_D-DC_DATA | 1_SATA_Tx- | 1_USB2- | 1_PE_Tx00- | V_IO | GND |
| 3 | GND | GNT4# | REQ4# | GNT3# | GND | CLK4 | GND |
| 2 | GND | REQ3# | GNT2# | - | CLK3 | CLK2 | GND |
| 1 | GND | REQ2# | GNT1# | REQ1# | GND | CLK1 | GND |

Note: SATA ports 3 and 4 support SATA revision 3.x (6.0 Gb/s). The second Ethernet interface (marked in gray) can be implemented as an option on a special board version.

***Table 14.*** *Signal mnemonics of CompactPCI connector J2 – CompactPCI and CompactPCI PlusIO rear I/O*

| | Signal | Direction | Function |
|---|---|---|---|
| **CompactPCI** | CLK[6:1] | out | Clocks 1 to 6 |
| | PBRST# | in | Push button reset |
| | DEG# | in | Power supply degenerate |
| | FAIL# | in | Power supply fail |
| | PWRBTN# | in | Power button |
| | REQ#/GNT#[6:1] | in/out | Request/grant pairs 1 to 6 |
| **Ethernet** | 1_ETH_A+, 1_ETH_A- | in/out | Differential data pair 0, Ethernet port 1 |
| | 1_ETH_B+, 1_ETH_B- | in/out | Differential data pair 1, Ethernet port 1 |
| | 1_ETH_C+, 1_ETH_C- | in/out | Differential data pair 2, Ethernet port 1 |
| | 1_ETH_D+, 1_ETH_D- | in/out | Differential data pair 3, Ethernet port 1 |
| | 2_ETH_A+, 2_ETH_A- | in/out | Differential data pair 0, Ethernet port 2 (instead of one interface at the front) |
| | 2_ETH_B+, 2_ETH_B- | in/out | Differential data pair 1, Ethernet port 2 (instead of one interface at the front) |
| | 2_ETH_C+, 2_ETH_C- | in/out | Differential data pair 2, Ethernet port 2 (instead of one interface at the front) |
| | 2_ETH_D+, 2_ETH_D- | in/out | Differential data pair 3, Ethernet port 2 (instead of one interface at the front) |

| | Signal | Direction | Function |
|---|---|---|---|
| **SATA** | 1_SATA_Rx+, 1_SATA_Rx- | in | Differential pair of SATA receive lines, port 1 |
| | 1_SATA_Tx+, 1_SATA_Tx- | out | Differential pair of SATA transmit lines, port 1 |
| | 2_SATA_Rx+, 2_SATA_Rx- | in | Differential pair of SATA receive lines, port 2 |
| | 2_SATA_Tx+, 2_SATA_Tx- | out | Differential pair of SATA transmit lines, port 2 |
| | 3_SATA_Rx+, 3_SATA_Rx- | in | Differential pair of SATA receive lines, port 3 (SATA revision 3.x support) |
| | 3_SATA_Tx+, 3_SATA_Tx- | out | Differential pair of SATA transmit lines, port 3 (SATA revision 3.x support) |
| | 4_SATA_Rx+, 4_SATA_Rx- | in | Differential pair of SATA receive lines, port 4 (SATA revision 3.x support) |
| | 4_SATA_Tx+, 4_SATA_Tx- | out | Differential pair of SATA transmit lines, port 4 (SATA revision 3.x support) |
| **SGPIO** | SATA_SC | out | Clock signal |
| | SATA_SL | out | Last clock of a bit stream; begin a new bit stream on the next clock |
| | SATA_SDO | out | Serial data output bit stream |
| | SATA_SDI | in | Serial data input bit stream (may not be supported by all SGPIO devices) |
| **USB** | 1_USB2+, 1_USB2- | in/out | Differential pair of USB lines, port 1 |
| | 2_USB2+, 2_USB2- | in/out | Differential pair of USB lines, port 2 |
| | 3_USB2+, 3_USB2- | in/out | Differential pair of USB lines, port 3 |
| | 4_USB2+, 4_USB2- | in/out | Differential pair of USB lines, port 4 |

| | Signal | Direction | Function |
|---|---|---|---|
| **PCI Express** | 1_PE_Rx00+, 1_PE_Rx00- | in | Differential PCIe receive lines, lane 1 |
| | 1_PE_Tx00+, 1_PE_Tx00- | out | Differential PCIe transmit lines, lane 1 |
| | 2_PE_Rx00+, 2_PE_Rx00- | in | Differential PCIe receive lines, lane 2 |
| | 2_PE_Tx00+, 2_PE_Tx00- | out | Differential PCIe transmit lines, lane 2 |
| | 3_PE_Rx00+, 3_PE_Rx00- | in | Differential PCIe receive lines, lane 3 |
| | 3_PE_Tx00+, 3_PE_Tx00- | out | Differential PCIe transmit lines, lane 3 |
| | 4_PE_Rx00+, 4_PE_Rx00- | in | Differential PCIe receive lines, lane 4 |
| | 4_PE_Tx00+, 4_PE_Tx00- | out | Differential PCIe transmit lines, lane 4 |
| | [1:4]_PE_CLKE# | in | Presence detect, PCIe lane 1..4 |
| | [1:4]_PE_CLK-, [1:4]_PE_CLK+ | out | Differential 100 MHz Reference Clock, PCIe lane 1:4 |
| **VGA (optional on special conduction-cooled board version)** | CRT_R_DDC_CLK | | Display Data Channel clock |
| | CRT_R_DDC_DATA | | Display Data Channel data lines |

### 2.16.4 Power Supply Status (*DEG#*, *FAIL#*)

Power supply failures may be detected before the system crashes down by monitoring the signals *DEG#* or *FAIL#*. These active-low lines are additions of the CompactPCI specification and may be driven by the power supply. *DEG#* signals the degrading of the supply voltages, *FAIL#* their possible failure.

## 2.17 Reset Button and Status LED

The F22P has a reset button and one status LED at the front panel. The reset button is recessed within the front panel and requires a tool, e.g. paper clip to be pressed, preventing the button from being inadvertently activated.

The yellow status LED shows board status messages. The LED is controlled by the board controller. It is switched on when the BIOS starts, switched off when the board is switched off and flashing slowly when the board is in stand-by (S3) status.

During normal operation the LED can be switched on and off using the MEN driver for the board controller.

See MEN's website for further information.

In case of a board failure, the LED displays the following error messages:

***Table 15.*** *Error codes signaled by board management controller via LED flashes*

| Number of Flashes | Error | Description |
|---|---|---|
| 0 | *CPUBCI_ERR_NONE* | No error |
| 1 | *CPUBCI_ERR_33V* | 3.3 V failure |
| 2 | *CPUBCI_ERR_INP* | Input voltage failure |
| 3 | *CPUBCI_ERR_NO_EXT_PWR_OK* | External power supply failure |
| 4 | *CPUBCI_ERR_CPU_TOO_HOT* | CPU temperature too high |
| 5 | *CPUBCI_ERR_BIOS_TIMEOUT* | BIOS startup failure |
| >5 | | Internal error |

## 2.18 SMBus Devices

***Table 16.*** *SMBus devices*

| Address[1] | Function |
|---|---|
| 0x9A / 0x9B | Board controller |
| 0xA0 | Memory channel A |
| 0x60 | Protected register |
| 0x30 | Temperature sensor A |
| 0xA4 | Memory channel B |
| 0x64 | Protected register |
| 0x34 | Temperature sensor B |
| 0xAE | Board EEPROM |
| 0x6E | Protected register |
| 0x3E | Temperature sensor B |

[1] The first address is for write command, the second for read command

# 3 BIOS

## 3.1 InsydeH2O Framework

The F22P is equipped with an InsydeH2O setup utility from Insyde Software. InsydeH2O is Insyde Software's firmware product line designed to replace traditional PC BIOS. It is an implementation of the Intel's Platform Innovation Framework for UEFI/EFI. The UEFI/EFI specification defines a new model for the interface between operating systems and platform firmware. This interface consists of data tables that contain platform-related information, plus boot and runtime service calls that are available to the operating system and its loader. Together, these provide a standard environment for booting an operating system and running pre-boot applications. This product line is the next generation of PC BIOS technology.

## 3.2 Accessing the Firmware

Even if you do not make any changes in the firmware, it can be useful to access the settings.

You can access the firmware at start-up of the F22P using your keyboard and screen connected at the board’s front panel by pressing <F2> immediately after boot-up.

## 3.3 UEFI Firmware System Setup Utility

The F22P UEFI firmware comes with a Setup Configuration Utility (SCU), simply called "system setup", as commonly known.

The ">" character in front of a menu item means that a sub-menu is available. An "x" in front of a menu item means that there is a configuration option which needs to be activated through a higher configuration option before being accessible.

The F22P BIOS has two configuration modes. One mode shows only a selection of the most important items and hides items where normally no changes in the settings are required. This manual only describes the short mode. You can easily switch between the two modes via a menu item Full Configuration Mode.

The settings shown in the following description are usually the default settings.

## 3.4 Main

| InsydeH2O Setup Utility | | | | | Rev. 3.5 |
|---|---|---|---|---|---|
| Main | Advanced | Security | Power | Boot | Exit |

| | |
|---|---|
| InsydeH2O Version | F21P/F22P 1.06 |
| Processor Type | Genuine Intel(R) CPU @ 2.40 GHz |
| System Bus Speed | 100 MHz |
| System Memory Speed | 1333 MHz |
| MEN BMC Rev | 1.5.0 |
| MEN Board Model/Rev | Not detected |
| MEN Board S/N | 2344 |
| Cache RAM | 1024kB |
| Total Memory | 4096MB |
| Channel A | |
| SODIMM 0 | 2048 MB |
| SODIMM 1 | [Not installed] |
| Channel B | |
| SODIMM 0 | 2048 MB |
| SODIMM 1 | [Not installed] |
| Platform Configuration | |
| CPU ID: | 0x306A9 |
| Microcode Rev: | 0x15 |
| Number of Core: | 2 |
| Number of Thread: | 4 |
| SMX/TXT: | Supported |
| VT-d: | Supported |
| VMX: | Supported |
| PCH-Rev: | 04 (PPT-C1 Stepping) |
| VBIOS Version: | 2137 |
| Intel ME Version: | 8.1.20.1336 |
| SA-Rev: | 09 (E1 Stepping) |
| Language | [English] |
| System Time | [hh:mm:ss] |
| System Date | [mm/dd/yyyy] |
| | |
| About this Software | |
| Full configuration mode | [No] |

| | InsydeH2O Setup Utility | | Rev. 3.5 |
|---|---|---|---|
| F1 Help | ↑↓ Select Item | F5/F6 Change Values | F9 Setup Defaults |
| Esc Exit | ← → Select Menu | Enter Select > Submenu | F10 Save and Exit |

### InsydeH2O Version / Processor Type / System Bus Speed / System Memory Speed/MEN Board Rev/ MEN BMC Rev / MEN Board Rev/ MEN Board S/N/ Cache RAM/ Total Memory / SODIMM 0 / SODIMM 1/Platform Configuration/CPU ID/Microcode Rev/Number of Core/Number of Thread/SMX/TXT/VT-d/VMX/PCH-Rev/VBIOS Version/Intel ME Version/ SA-Rev

| | |
|---|---|
| **Description** | You cannot change any values in these fields. They are only for information. |

### Language

| | | |
|---|---|---|
| **Description** | Select the default language | |
| **Options** | *English* | |

### System Time

| | | |
|---|---|---|
| **Description** | Change the internal clock. | |
| **Options** | *hh* | Hours (Valid range from 0 to 23) |
| | *mm* | Minutes (Valid range from 0 to 59) |
| | *ss* | Seconds (Valid range from 0 to 59) |

### System Date

| | | |
|---|---|---|
| **Description** | Change the date | |
| **Options** | *mm* | Month (Valid range from 1 to 12) |
| | *dd* | Day (Valid range from 1 to 31) |
| | *yyyy* | Year (Valid range from 2000 to 2099) |

### Full Configuration Mode

| | | |
|---|---|---|
| **Description** | The F22P BIOS has two configuration modes. One mode shows only a selection of the most important items and hides items where normally no changes in the settings are required. | |
| **Options** | *Yes* | Enable full configuration mode |
| | *No* | Disable full configuration mode |

## 3.5 Advanced

| InsydeH2O Setup Utility | | | | | | Rev. 3.5 |
|---|---|---|---|---|---|---|
| Main | Advanced | Security | Power | Boot | Exit | |
| >Boot Configuration | | | | | | |
| >Peripheral Configuration | | | | | | |
| >IDE Configuration | | | | | | |
| >Thermal Configuration | | | | | | |
| >Video Configuration | | | | | | |
| >USB Configuration | | | | | | |
| >Chipset Configuration | | | | | | |
| >ACPI Table/Features Control | | | | | | |
| >Active Management Technology Support | | | | | | |
| >PCI Express Configuration | | | | | | |
| F1 Help | ↑↓ Select Item | | | F5/F6 Change Values | | F9 Setup Defaults |
| Esc Exit | ← → Select Menu | | | Enter Select > Submenu | | F10 Save and Exit |

### Boot Configuration — Sub-menu

```
SCU Resolution            [1024 x 768]
SATA port on sidecard     [Port B]
Add additional delay
during BIOS boot process  [No delay]
Power Supply Type         [ATX]
Watchdog                  [Off]
PWRON after PWR-Fail      [On]
ATX_PWRGD Failure Mode    [Check at Start-Up]
External PS Control       [Switched]
Platform Reset Management [RESET_IN is enabled]
```

#### SCU Resolution

| | | |
|---|---|---|
| **Description** | Change resolution of setup utility. | |
| **Options** | *640 x 480* | *800 x 600* |
| | *1024 x 768* | |

#### SATA port on side card

| | | |
|---|---|---|
| **Description** | Selects the SATA port on the sidecard. | |
| **Options** | *Port A* | *Port B* |

#### Add additional delay during BIOS boot process

| | | |
|---|---|---|
| **Description** | Helpful for init delay of peripheral boards | |
| **Options** | *No delay* | *100 ms delay* |
| | *200 ms delay* | *300 ms delay* |
| | *400 ms delay* | *500 ms delay* |
| | *600 ms delay* | *700 ms delay* |
| | *800 ms delay* | |

#### Power Supply Type

| | | |
|---|---|---|
| **Description** | Selects the type of power supply | |
| **Options** | *AT* | *ATX* |

#### Watchdog

| | | |
|---|---|---|
| **Description** | Enables or disables the F22P Watchdog | |
| **Options** | *Off* | *10 min* |
| | *1 min* | *15 min* |
| | *2 min* | *20 min* |
| | *5 min* | *30 min* |

#### PWRON after PWR-Fail

| | | |
|---|---|---|
| **Description** | Sets the system power status when power returns to the system from a power failure situation. | |
| **Options** | *On* | *Off* |
| | *Former State* | |

| ATX_PWRGD Failure Mode | | |
|---|---|---|
| **Description** | Determines the system behavior in case of a failure at the ATX power good signal | |
| **Options** | *Check at Start-Up* | *Check always* |

| External PS Control | | |
|---|---|---|
| **Description** | Controls the external Power Supply | |
| **Options** | *Always on* | *Switched* |

| Platform Reset Management | | |
|---|---|---|
| **Description** | Enables or blocks the RESET_IN signal of the board. | |
| **Options** | *RESET_IN is enabled* | *RESET_IN is blocked* |

### Peripheral Configuration — Sub-menu

```
Azalia              [Disabled]
LAN-1               [Enabled]
LAN-2               [Enabled]
LAN-3               [Enabled]
Workaround for MEN F223 [Disabled]
```

| | | |
|---|---|---|
| **Azalia** | | |
| **Description** | Enables or disables the Audio controller. | |
| **Options** | *Auto* | The controller is enabled if a codec is found. |
| | *Disabled* | The controller is disabled even when there is an audio codec. |
| | *Enabled* | The controller is enabled independent of the presence of a codec. |
| **LAN-1** | | |
| **Description** | Enables or disables Intel 82579 GbE (AMT). | |
| **Options** | *Enabled* | *Disabled* |
| **LAN-2** | | |
| **Description** | Enables or disables Intel I211 GbE | |
| **Options** | *Enabled* | *Disabled* |
| **LAN-3** | | |
| **Description** | Enables or disables the LAN-3 controller | |
| **Options** | *Enabled* | *Disabled* |
| **Workaround for MEN F223** | | |
| **Description** | Enables or disables workaround for F223 PCI detection. Necessary for Windows operating system. | |
| **Options** | *Enabled* | *Disabled* |

### IDE Configuration — Sub-menu

```
IDE Controller                      [Enabled]
HDC Configure as                    [AHCI]
>Software Feature Mask Configuration

    HDD Unlock                      [Enabled]
    LED Locate                      [Enabled]

Aggressive LPM Support              [Enabled]
SATA Port 0                         [Enabled]
  SATA Port Hot Plug                [Disabled]
  Spin-Up Device                    [Disabled]
  SATA Device Type                  [Hard Disk Drive]
  Port Multiplier                   [Disabled]
SATA Port 1                         [Enabled]
  SATA Port Hot Plug                [Disabled]
  Spin-Up Device                    [Disabled]
  SATA Device Type                  [Hard Disk Drive]
  Port Multiplier                   [Disabled]
SATA Port 2                         [Enabled]
  SATA Port Hot Plug                [Disabled]
  Spin-Up Device                    [Disabled]
  SATA Device Type                  [Hard Disk Drive]
  Port Multiplier                   [Disabled]
SATA Port 3                         [Enabled]
  SATA Port Hot Plug                [Disabled]
  Spin-Up Device                    [Disabled]
  SATA Device Type                  [Hard Disk Drive]
  Port Multiplier                   [Disabled]
SATA Port 4                         [Enabled]
  SATA Port Hot Plug                [Disabled]
  Spin-Up Device                    [Disabled]
  SATA Device Type                  [Hard Disk Drive]
  Port Multiplier                   [Disabled]
SATA Port 5                         [Enabled]
  SATA Port Hot Plug                [Disabled]
  Spin-Up Device                    [Disabled]
  SATA Device Type                  [Hard Disk Drive]
  Port Multiplier                   [Disabled]
```

#### IDE Controller

**Description** Enables or disables the IDE controllers.

**Options** *Enabled* *Disabled*

#### HDC Configure as

**Description** Set hard disk controller configure type.

**Options** *IDE* *RAID*
*AHCI*

#### > Software Feature Mask Configuration

The RAID OROM/RST driver will refer to SWFM configuration to enable/disable the storage feature

#### HDD Unlock

| | | |
|---|---|---|
| **Description** | Enables or disables the unlock button for protected drives in the Intel RST manager. | |
| **Options** | *Enabled* | *Disabled* |
| **LED Locate** | | |
| **Description** | If enabled, it is indicated that the LED/SGPIO hardware is attached and the pin to locate the feature is enabled in the OS. | |
| **Options** | *Enabled* | *Disabled* |
| **Aggressive LPM support** | | |
| **Description** | Enables or disables aggressive LPM support. | |
| **Options** | *Enabled* | *Disabled* |
| **SATA Port 0/1/2/3/4/5** | | |
| **Description** | Enables or disables SATA ports. | |
| **Options** | *Enabled* | *Disabled* |
| **SATA Port Hot Plug** | | |
| **Description** | Enables or disables the SATA Port Hot Plug feature. | |
| **Options** | *Enabled* | *Disabled* |
| **Spin-up Device** | | |
| **Description** | Enables or disables Spin-up device. | |
| **Options** | *Enabled* | *Disabled* |
| **SATA Device Type** | | |
| **Description** | Selects the SATA device. | |
| **Options** | *Hard Disk Drive* | *Solid State Drive* |
| **Port Multiplier** | | |
| **Description** | Enables or disables port multiplier. | |
| **Options** | *Enabled* | *Disabled* |

### Thermal Configuration — Sub-menu

```
>Platform Thermal Configuration

     Shut Down Temperature      [100°C]
     Throttle on Temperature    [85°C]

>CPU Thermal Configuration

     DTS                        [Enabled]
     Bidirectional PROCHOT#     [Disabled]
     ACPI 3.0 T-States          [Disabled]
```

#### Shut Down Temperature

| | | |
|---|---|---|
| **Description** | ACPI Critical Trip Point - the point at which the OS will shut down the system. | |
| **Options** | *70°C* | *75°C* |
| | *80°C* | *85°C* |
| | *90°C* | *100°C* |
| | *110°C* | *120°C* |

#### Throttle on Temperature

| | | |
|---|---|---|
| **Description** | Set the CPU temperature point of Throttle on. | |
| **Options** | *40°C* | *45°C* |
| | *50°C* | *55°C* |
| | *60°C* | *65°C* |
| | *70°C* | *75°C* |
| | *80°C* | *85°C* |
| | *90°C* | |

#### DTS

| | | |
|---|---|---|
| **Description** | Enables CPU Digital Thermal Sensor function. Out of spec: ACPI Thermal Management uses EC reported temperature values and DTS SMM is used to handle Out of Spec condition. | |
| **Options** | *Critical reporting* | *Disabled* |
| | *Enabled* | |

#### Bidirectional PROCHOT#

| | | |
|---|---|---|
| **Description** | This value cannot be changed. | |
| **Options** | *Disabled* | |

#### ACPI 3.0 T-States

| | | |
|---|---|---|
| **Description** | Enable or disable ACPI 3.0 T-States | |
| **Options** | *Disabled* | *Enabled* |

### Video Configuration — Sub-menu

```
Primary Display                [Auto]

>Internal Graphic Device

    Internal Graphics Device   [Auto]
    IGD - Gtt Size             [2 MB]
    IGD - Aperture Size        [256 MB]
    IGD - DVMT Pre-Allocated   [64 MB]
```

#### Primary Display

| | | |
|---|---|---|
| **Description** | Selects Primary Display Mode. | |
| **Options** | *Auto* | *IGFX* |
| | *PEG* | *PCI* |

#### Internal Graphics Device

| | | |
|---|---|---|
| **Description** | Enables or disables the Internal Graphics Device (IGD). | |
| **Options** | *Enabled* | *The IGD is enabled in any case.* |
| | *Disabled* | *The IGD is disabled* |
| | *Auto* | *The IGD is enabled only when a monitor is found* |

#### IGD – Gtt Size

| | | |
|---|---|---|
| **Description** | Selects the size of the Gtt (graphics translation table) memory. | |
| **Options** | *1 MB* | *2 MB* |

#### IGD – Aperture Size

| | | |
|---|---|---|
| **Description** | Selects the size of the system memory that is used by the Internal Graphics Device. | |
| **Options** | *128 MB* | *256 MB* |
| | *512 MB* | |

#### IGD - DVMT Pre-Allocated

| | | |
|---|---|---|
| **Description** | Select DVMT Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device. | |
| **Options** | *0 MB* | *32 MB* |
| | *64 MB* | *96 MB* |
| | *128 MB* | *160 MB* |
| | *192 MB* | *224 MB* |
| | *256 MB* | *288 MB* |
| | *320 MB* | *352 MB* |
| | *384 MB* | *416 MB* |
| | *448 MB* | *480 MB* |
| | *512 MB* | *1024 MB* |

### USB Configuration — Sub-menu

```
USB BIOS Support          [Enabled]
EHCI 1                    [Enabled]
EHCI 2                    [Enabled]
Pre-Port Control          [Disabled]
```

#### USB BIOS Support

| | | |
|---|---|---|
| **Description** | If this menu item is enabled it is possible to boot from USB devices and use a USB keyboard under DOS. Cannot be changed. No BIOS setup is possible if this item is not enabled. | |
| **Options** | *Enabled* | |

#### EHCI 1/2

| | | |
|---|---|---|
| **Description** | Enable/Disable EHCI 1/2. | |
| **Options** | *Enabled* | *Disabled* |

#### Pre-Port Control

| | | |
|---|---|---|
| **Description** | Enable/Disable the pre-port disable control override. | |
| **Options** | *Enabled* | *Disabled* |

### Chipset Configuration

```
Setup warning
Setting items on this screen to incorrect values may cause your system
to malfunction!

VT-d                      [Enabled]
```

#### VT-d

| | | |
|---|---|---|
| **Description** | Check to enable the VT-d (Intel Virtualization Technology for Directed I/O) function. | |
| **Options** | *Enabled* | *Disabled* |

### ACPI Table/Feature Control

```
FACP - RTC S4 Wakeup     [Enabled]
APIC - IO APIC Mode      [Enabled]
TCO Watchdog Support     [Enabled]
Watchdog ACPI Table      [Enabled]
```

#### FACP - RTC S4 Wakeup

| | | |
|---|---|---|
| **Description** | Value only for ACPI. Enable/Disable for S4 Wakeup from RTC. | |
| **Options** | *Enabled* | *Disabled* |

#### APIC - IO APIC Mode

| | | |
|---|---|---|
| **Description** | This item is valid only for WIN2k and WINXP.Also, a fresh install of the OS must occur when APIC Mode is desired.Test the IO ACPI by setting item to Enable.The APIC Table will then be pointed to by the RSDT, the Local APIC will be initialized, and the proper enable bits will be set in chipset. | |
| **Options** | *Enabled* | *Disabled* |

#### TCO Watchdog Support

| | | |
|---|---|---|
| **Description** | Enables or disables TCO Watchdog Support. | |
| **Options** | *Enabled* | *Disabled* |

#### Watchdog ACPI Table

| | | |
|---|---|---|
| **Description** | Enables or disables Watchdog ACPI Table. | |
| **Options** | *Enabled* | *Disabled* |

### Active Management Technology Support

```
Intel AMT Support              [Enabled]
```

#### Intel AMT Support

| | | |
|---|---|---|
| **Description** | Enable/disable Intel Active Management Technology BIOS extension. Note: iAMT H/W is always enabled. This option just controls the BIOS extension execution. | |
| **Options** | *Enabled* | *Disabled* |

### PCI Express Configuration

```
PCIE Port assigned to LAN      2

>PCI Express Root Port 1

  PCI Express Root Port 1       [Enabled]

>PCI Express Root Port 2
>PCI Express Root Port 3
>PCI Express Root Port 4
>PCI Express Root Port 5
>PCI Express Root Port 6
>PCI Express Root Port 7
```

#### PCIE Port assigned to LAN

| | |
|---|---|
| **Description** | Determines the number of the PCI Express port which is assigned to the LAN interface. |
| **Options** | *2* |

#### PCI Express Root Port 1/2/3/4/5/6/7

| | | |
|---|---|---|
| **Description** | Enables or disables PCI Express ports. If PCI Express Root Port 1 is disabled, PCI Express Root Ports 2 to 7 will also be disabled. | |
| **Options** | *Enabled* | *Disabled* |

## 3.6 Security

| InsydeH2O Setup Utility | | | | | | Rev. 3.5 |
|---|---|---|---|---|---|---|
| Main | Advanced | Security | Power | Boot | Exit | |
| TPM Status | | | Enabled and Active | | | |
| TPM Operation | | | [No Operation] | | | |
| TPM Force Clear | | | [Disabled] | | | |
| Supervisor Password | | | [Installed/Not Installed] | | | |
| Set Supervisor Password | | | | | | |
| F1 Help | | ↑↓ Select Item | | F5/F6 Change Values | | F9 Setup Defaults |
| Esc Exit | | ← → Select Menu | | Enter Select > Submenu | | F10 Save and Exit |

### TPM Status

| | |
|---|---|
| **Description** | Shows TPM (Trusted Platform Module) status. No changes can be made in this field. It is only for information. |
| **Options** | *Enabled and Active* |

### TPM Operation

| | |
|---|---|
| **Description** | TPM (Trusted Platform Module) operation. The TPM module can be used if the status is *Enable and Activate.* |
| **Options** | *No operation* *Disable and Deactivate* *Enable and Activate* |

### TPM Force Clear

| | |
|---|---|
| **Description** | Clear the TPM (Trusted Platform Module). TPM Force Clear is independent of the item TPM Operation. If set to *Enabled* the BIOS clears the TPM module at the next boot process (independent of whether it is activated or not). Clearing the TPM resets the TPM to an unowned state. After clearing the TPM, you need to complete the TPM initialization process before using software that relies on the TPM, such as BitLocker Drive Encryption. |
| **Options** | *Enabled* *Disabled* |

For more information regarding TPM see Chapter 5.1 Literature and Web Resources on page 79.

### Supervisor Password

| | |
|---|---|
| **Description** | Shows whether a supervisor password has been entered. |

### Set Supervisor Password

| | |
|---|---|
| **Description** | Enter and confirm the supervisor password under this menu item.<br>To delete the password enter an empty password. |

## 3.7 Power

| InsydeH2O Setup Utility | | | | | | Rev. 3.5 |
|---|---|---|---|---|---|---|
| Main | Advanced | Security | Power | Boot | Exit | |
| >Advanced CPU Control | | | | | | |
| Wake on Lan | | | [Disabled] | | | |
| F1 Help | | ↑↓ Select Item | | F5/F6 Change Values | | F9 Setup Defaults |
| Esc Exit | | ← → Select Menu | | Enter Select > Submenu | | F10 Save and Exit |

### Advanced CPU Control – Sub-Menu

```
P-States(IST)             [Enabled]
Active Processor Cores    [All Cores]
HT Support                [Auto]
VT Support                [Disabled]
Max CPUID Value Limit     [Disabled]

C-States                  [Enabled]
Enhanced C-States         [Enabled]

Turbo Mode                [Disabled]
```

#### P-States (IST)

| | | |
|---|---|---|
| **Description** | Enable processor performance states (P-States). | |
| **Options** | *Enabled* | *Disabled* |

#### Active Processor Cores

| | | |
|---|---|---|
| **Description** | Selects the number of active processor cores. | |
| **Options** | *All Core* | *1 Core* |
| | *2 Core* | *3 Core* |

#### HT Support

| | | |
|---|---|---|
| **Description** | Enable or disable Hyper Threading. | |
| **Options** | *Auto* | *Disabled* |

#### VT Support

| | |
|---|---|
| **Description** | Enable or disable Vanderpool technology. |

| | | |
|---|---|---|
| **Options** | *Enabled* | *Disabled* |

**Max CPUID Value Limit**

| | | |
|---|---|---|
| **Description** | Enable or disable Max CPUID Value Limit. | |
| **Options** | *Enabled* | *Disabled* |

**C-States**

| | | |
|---|---|---|
| **Description** | Enable processor idle power saving states (C-States). | |
| **Options** | *Enabled* | *Disabled* |

**Enhanced C-States**

| | | |
|---|---|---|
| **Description** | Enable P-State transitions to occur in combination with C-States. | |
| **Options** | *Enabled* | *Disabled* |

**Turbo Mode**

| | | |
|---|---|---|
| **Description** | Enables/disables processor turbo mode (the EMTTM feature has to be enabled too) | |
| **Options** | *Enabled* | *Disabled* |

### Wake on Lan

| | | |
|---|---|---|
| **Description** | Determines the action taken when the system power is off and a Wake on Lan event occurs. | |
| **Options** | *Enabled* | *Disabled* |

## 3.8 Boot

| InsydeH2O Setup Utility | | | | | Rev. 3.5 |
|---|---|---|---|---|---|
| Main | Advanced | Security | Power | Boot | Exit |
| Boot Type | | | [Dual Boot Type] | | |
| Quick Boot | | | [Enabled] | | |
| Quiet Boot | | | [Enabled] | | |
| Network Stack | | | [Disabled] | | |
| PXE Boot Capability | | | [Disabled] | | |
| Add Boot Options | | | [Auto] | | |
| ACPI Selection | | | [ACPI 5.0] | | |
| USB Boot | | | [Enabled] | | |
| EFI Device First | | | [Disabled] | | |
| Timeout | | | [0] | | |
| Automatic Failover | | | [Disabled] | | |
| >EFI | | | | | |
| F1 Help | | ↑↓ Select Item | | F5/F6 Change Values | F9 Setup Defaults |
| Esc Exit | | ← → Select Menu | | Enter Select > Submenu | F10 Save and Exit |

### Boot Type

| | |
|---|---|
| **Description** | Determines the boot type. |
| **Options** | *Dual Boot Type* *Legacy Boot Type* *UEFI Boot Type* |

### Quick Boot

| | |
|---|---|
| **Description** | Allows InsydeH2O to skip certain tests while booting. This will decrease the time needed to boot the system. |
| **Options** | *Enabled* *Disabled* |

### Quiet Boot

| | |
|---|---|
| **Description** | Disables or enables booting in Text Mode |
| **Options** | *Enabled* *Disabled* |

### Network Stack

| | | |
|---|---|---|
| **Description** | Network Stack Support: Windows 8, Bitlocker Unlock, UEFI IPv4/ IPv6 PXE, Legacy PXE OPROM | |
| **Options** | *Enabled* | *Disabled* |

### PXE Boot Capability

| | | |
|---|---|---|
| **Description** | Disables or enables PXE boot to LAN. Cannot be changed. | |
| **Options** | *Disabled* | |

### Add Boot Options

| | | |
|---|---|---|
| **Description** | Position in boot order for shell, network and removables. | |
| **Options** | *Auto* | *First* |
| | *Last* | |

### ACPI Selection

| | | |
|---|---|---|
| **Description** | Select booting to Acpi4.0/Acpi5.0 | |
| **Options** | Acpi5.0 | Acpi4.0 |

### USB Boot

| | | |
|---|---|---|
| **Description** | Disables or enables booting to USB boot devices. | |
| **Options** | *Enabled* | *Disabled* |

### EFI Device First

| | | |
|---|---|---|
| **Description** | Determines whether the EFI device or the legacy device is booted first. If enabled the EFI device is booted first. If disabled the legacy device is booted first. | |
| **Options** | *Enabled* | *Disabled* |

### Timeout

| | |
|---|---|
| **Description** | The number of seconds that the firmware will wait before booting the original default boot selection. |
| **Options** | *0* |

### Automatic Failover

| | | |
|---|---|---|
| **Description** | Enable: if boot to default device fails, it will directly try to boot next device.<br>Disable: if boot to default device fails, it will pop warning then go into firmware UI. | |
| **Options** | *Enabled* | *Disabled* |

### EFI – Sub-Menu

```
EFI

Internal EFI Shell
```

**EFI Boot Menu**

**Description** Displays a list of EFI boot media.

## 3.9 Exit

| InsydeH2O Setup Utility | | | | | | Rev. 3.5 |
|---|---|---|---|---|---|---|
| Main | Advanced | Security | Power | Boot | Exit | |
| Exit Saving Changes | | | | | | |
| Save Change Without Exit | | | | | | |
| Exit Discarding Changes | | | | | | |
| Load Optimal Defaults | | | | | | |
| Load Custom Defaults | | | | | | |
| Save Custom Defaults | | | | | | |
| Discard Changes | | | | | | |
| F1 Help | | ↑↓ Select Item | | F5/F6 Change Values | | F9 Setup Defaults |
| Esc Exit | | ← → Select Menu | | Enter Select > Submenu | | F10 Save and Exit |

### 3.9.1 Exit Saving Changes

Exit system setup and save your changes.

### 3.9.2 Save Change Without Exit

Save your changes without exiting the system.

### 3.9.3 Exit Discarding Changes

Exit system setup without saving your changes.

### 3.9.4 Load Optimal Defaults

If this option is selected, a verified factory setup is loaded.

On the first BIOS setup configuration, this loads safe values for setup, which make the board boot up.

### 3.9.5 Load Custom Defaults

If this option is selected the custom defaults that have been saved in a former session with Save Custom Defaults are loaded.

Also see Chapter 3.9.6 Save Custom Defaults

### 3.9.6 Save Custom Defaults

Save custom defaults.

### 3.9.7 Discard Changes

Discard changes.

# 4 Maintenance

## 4.1 Lithium Battery

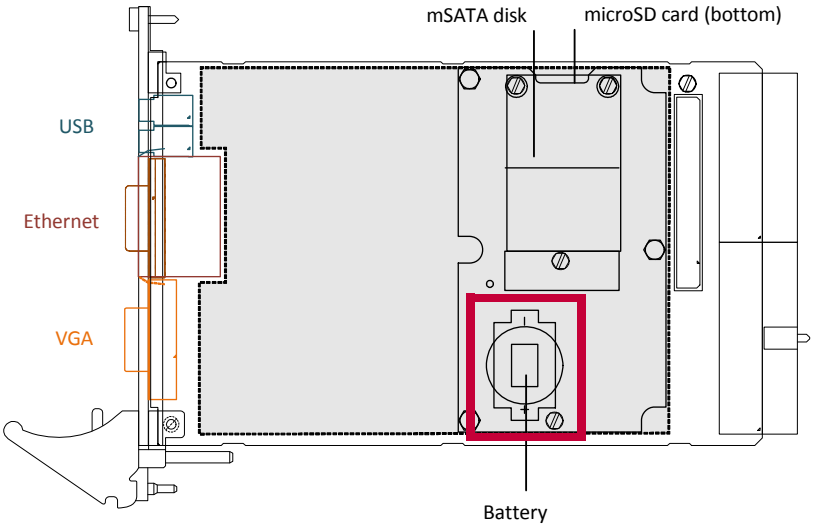
The board contains a lithium battery. There is a danger of explosion if the battery is incorrectly replaced!
Replace only with the same or equivalent type.

- Manufacturer: Renata
- Type: CR2032
- Capacity: 235 mAh

The battery has to be UL listed.

Used batteries have to be disposed of according to the local regulations concerning the disposal of hazardous waste.

***Figure 3.*** *Position of battery on the mass storage adapter on the F22P*



# 5 Appendix

## 5.1 Literature and Web Resources

F22P data sheet with up-to-date information and documentation

### 5.1.1 CPU

Intel Embedded Processors

### 5.1.2 TPM (Trusted Platform Module)

Trusted Computing Group: How to use the TPM

TPM Management under Windows

### 5.1.3 SATA

Serial ATA International Organization (SATA-IO)

### 5.1.4 USB

USB Implementers Forum, Inc.

### 5.1.5 Ethernet

ANSI/IEEE 802.3-1996, Information Technology - Telecommunications and Information Exchange between Systems - Local and Metropolitan Area Networks - Specific Requirements - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications; 1996; IEEE

Charles Spurgeon's Ethernet Web Site

InterOperability Laboratory, University of New Hampshire
This page covers general Ethernet technology.

### 5.1.6 HD Audio

Intel High Definition Audio

### 5.1.7 PCI Express

PCI Special Interest Group

### 5.1.8 CompactPCI

CompactPCI Specification PICMG 2.0 R3.0:
1999; PCI Industrial Computers Manufacturers Group (PICMG)

PCI Local Bus Specification Revision 2.2:
1995; PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214, USA

### 5.1.9 CompactPCI PlusIO

CompactPCI PlusIO Specification PICMG 2.30 R1.0:
2009; PCI Industrial Computers Manufacturers Group (PICMG)

Introduction to CompactPCI PlusIO on Wikipedia

## 5.2 Finding out the Product's Article Number, Revision and Serial Number

MEN user documentation may describe several different models and/or design revisions of the F22P. You can find information on the article number, the design revision and the serial number on a label attached to the board.

- **Article number:** Gives the product's family and model. This is also MEN's ordering number. To be complete it must have 9 characters.
- **Revision number:** Gives the design revision of the product.
- **Serial number:** Unique identification assigned during production.

If you need support, you should communicate these numbers to MEN.

***Figure 4.*** *Labels giving the product's article number, revision and serial number*