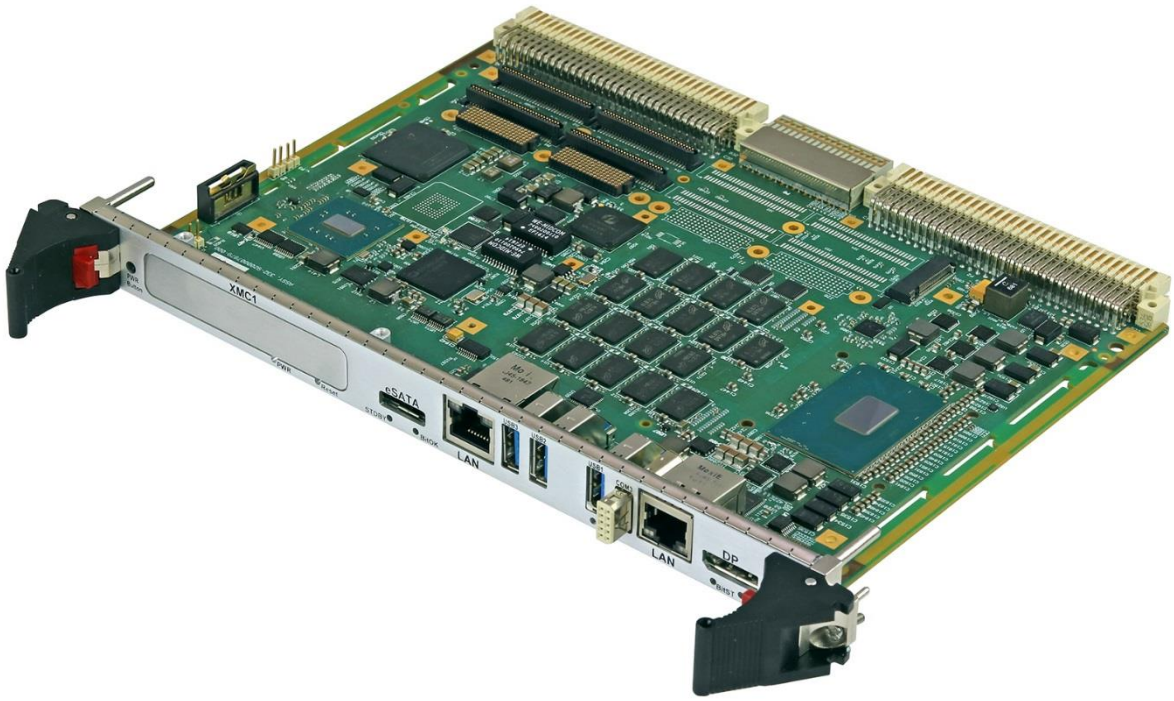
Hardware Reference Manual

XVB603 Intel® Xeon® Based VME Single Board Computer

THE XVB603 IS DESIGNED TO MEET THE EUROPEAN UNION (EU) RESTRICTIONS OF HAZARDOUS SUBSTANCE (ROHS) DIRECTIVE (2015/863) CURRENT REVISION.

Publication No. 500-9300007880-000 Rev. M



abaco SYSTEMS

Document History

Revision	Date	Description
A	September 2017	Initial Release
B	November 2017	Correct LED Control Register, Table 7-11.
C	February 2018	Update the block diagram and various small changes per changes to the datasheet.
D	February 2018	Update FPGA tables
E	March 2018	Add note to Appendix B regarding option-dependent connections. Add section in Appendix C to enable/disable sleep states.
F	April 2018	Adjusted contact reference for Programming the VME Controller FPGA.
G	July 2018	Attached Engineering redlines and email with changes needed to ECN Removed top assembly LEDs (covered by heatsink) Added LED DS439 to bottom assembly section
H	August 2018	Clarified front panel reference designators in Chapter 4.
J	August 2018	Clarified Write Protect settings for jumper header P6 on the XVB603 and P12 on the VTM29.
K	November 2018	Referenced M.2 support where applicable and reserved SSD support – currently not available on the XVB603.
L	June 2019	Sections 3.3.2, 5.7.3, C.6.2, C.6.5: Clarified the changing of settings in the DIP Switch menu of the BIOS. Section A.6.1: Added note to detail change in XVB603 max storage temp when battery is installed. Updated Section 5.7.1 Updated Table 4-16 (P2 pinout) to include XMC/PMC I/O signals on Rows A and C. Updated registers in Chapter 7.
M	October 2019	Added support for the XVB603 w/EXP238 board in Appendix E.

Waste Electrical and Electronic Equipment (WEEE) Returns

Abaco Systems is registered with an approved Producer Compliance Scheme (PCS) and, subject to suitable contractual arrangements being in place, will ensure WEEE is processed in accordance with the requirements of the WEEE Directive.

Abaco Systems will evaluate requests to take back products purchased by our customers before August 13, 2005 on a case by case basis. A WEEE management fee may apply.

About This Manual

Conventions

Notices

This manual may use the following types of notice:

WARNING

Warnings alert you to the risk of severe personal injury.

CAUTION

Cautions alert you to system danger or loss of data.

NOTE

Notes call attention to important features or instructions.

TIP

Tips give guidance on procedures that may be tackled in a number of ways.

LINK

Links take you to other documents or websites.

Numbers

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a “D” subscript and binary numbers have a “b” subscript. The prefix “0x” shows a hexadecimal number, following the ‘C’ programming language convention. Thus:

One dozen = 12_D = 0x0C = 1100_b

The multipliers “k”, “M” and “G” have their conventional scientific and engineering meanings of $x10^3$, $x10^6$ and $x10^9$, respectively, and can be used to define a transfer rate. The only exception to this is in the description of the size of memory areas, when “K”, “M” and “G” mean $x2^{10}$, $x2^{20}$ and $x2^{30}$ respectively.

In PowerPC terminology, multiple bit fields are numbered from 0 to n where 0 is the MSB and n is the LSB. PCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Text

Signal names ending with “#” denote active low signals; all other signals are active high. “-” and “+” denote the low and high components of a differential signal respectively.

Further Information

Abaco Website

You can find information regarding Abaco products on the following website:

LINK
https://www.abaco.com

Abaco Documents

This document is distributed via the Abaco website. You may register for access to manuals via the website.

LINK
https://www.abaco.com/download/xvb603-hardware-reference-manual

Third-party Documents

ANSI/VITA Standards

LINK
http://www.vita.com

Intel® Xeon Processor/CM238 Chipset

LINK
http://www.intel.com

IEEE Standards

LINK
http://www.ieee.com

IPC Standards

LINK
http://www.ipc.com

NOTE
Technical literature describing components used on the XVB603 is available from the manufacturers' websites.

Technical Support Contact Information

You can find technical assistance contact details on the website Support page.

LINK
https://www.abaco.com/support

Abaco will log your query in the Technical Support database and allocate it a unique Case number for use in any future correspondence.

Alternatively, you may also contact Abaco's Technical Support via:

LINK
support@abaco.com

Returns

If you need to return a product, there is a Return Materials Authorization (RMA) form available via the website Support page.

LINK
https://www.abaco.com/support

Do not return products without first contacting the Abaco Repairs facility.

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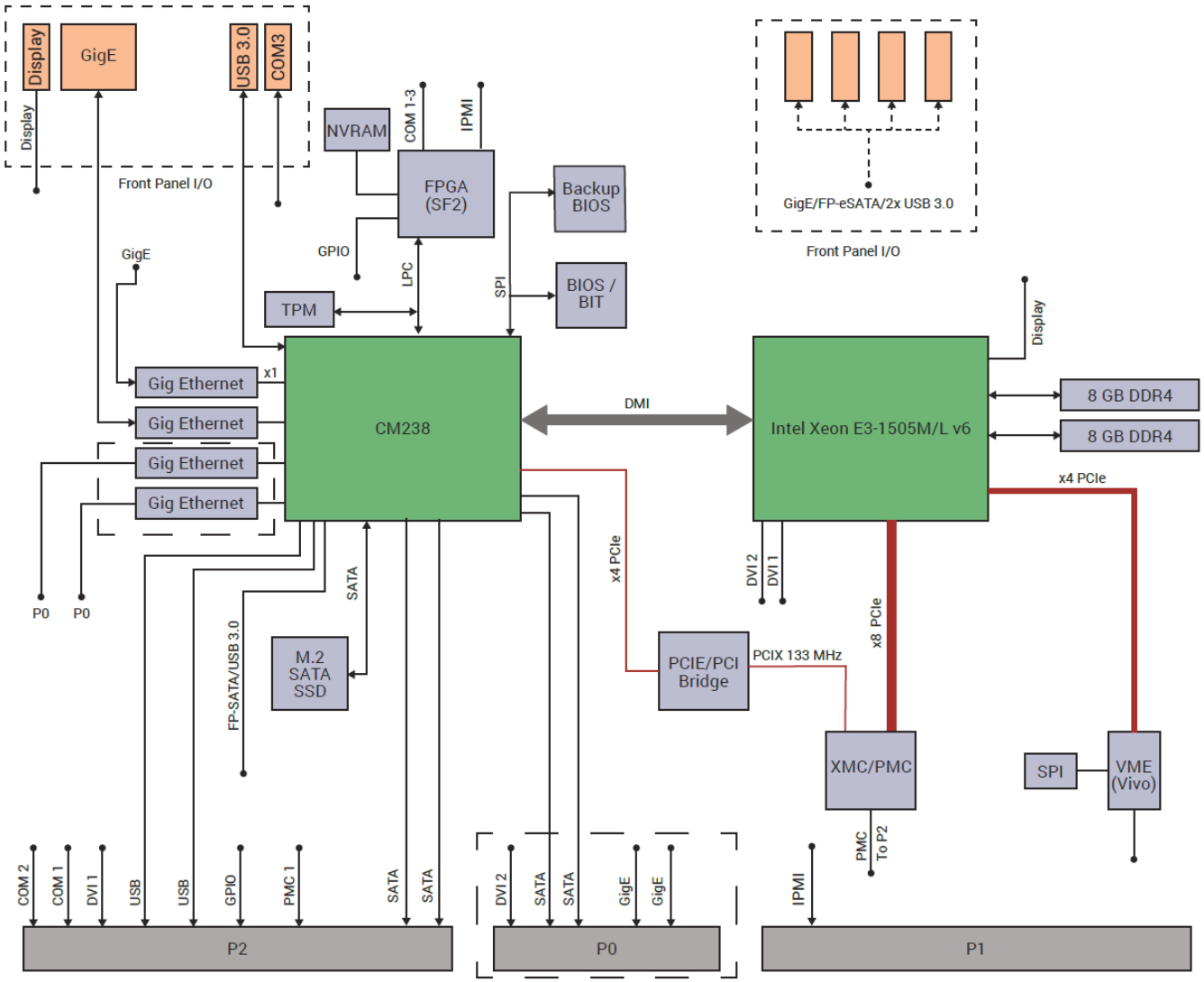
1 • Introduction

Abaco Systems' XVB603 6U VME Single Board Computer (SBC) features the Intel® Xeon® quad core processor (up to 8 MByte Last Level Cache) with error checking and correction (ECC) support, integrated graphics and PCI Express (PCIe) channels. The XVB603 is also equipped with Intel's CM238 Chipset, supporting PCIe Gen 3, allowing higher data transfer rates and more PCIe channels. The CM238 chipset also provides SATA, USB 3.0, graphic ports, SMBus, LPC and SPI design on the XVB603.

Figure 1-1 XVB603 Block Diagram



1.1 Features

- Single-slot 6U VME Single Board Computer
- Intel Xeon quad core processor
- Two channels of soldered DDR4 SDRAM with ECC up to 16 GByte
- Up to 8 MByte Internal CPU shared cache
- Up to 256 GBytes of removable SATA M.2 Flash (Optional)
- Onboard Expansion Site (supporting either XMC or PMC)
    - 1x XMC – x8 PCIe
    - 1x PMC – PCI-X up to 133 MHz
- XMC/PMC Expansion Board (EXP238) available via onboard XMC site (Only available on specific option of XVB603). See Appendix E for details on the EXP238 option.
    - 3x XMC – x4 PCIe
    - 1x PMC – PCI-X up to 133 MHz
    - 2x PMC – PCI-X up to 66 MHz
- Comprehensive range of front and rear I/O features:

1.1.1 Front I/O: (Option-Dependent)

- 2x Gigabit Ethernet ports via Intel I210
- 1x DisplayPort
- 3x USB 3.0 ports
- 1x COM port
- 1x Power button
- 1x eSATA

1.1.2 Rear I/O via Transition Module: (Option-Dependent)

- 2x Gigabit Ethernet ports
    - 1x Gigabit Ethernet via Intel I219
    - 1x Gigabit Ethernet via Intel I210
- 2x Digital Video Interface (DVI)
- 4x SATA ports, Gen 2 capable
- 2x COM ports
- 2x USB 2.0 ports
- 8x General Purpose Input/Output (GPIO)
- 1x PMC rear I/O
- 2x Mezzio connectors (PMC/XMC)

LINK

The VTM29 Rear Transition Module is compatible with the XVB603. See the product details on the Abaco website: https://www.abaco.com/download/vtm29-hardware-reference-manual.

1.1.3 Other Features

- UEFI Flash and UEFI backup Flash
- Optional extended operating temperature range
- Two levels of ruggedization

The XVB603 offers one optional onboard mezzanine expansion site for enhanced system flexibility, PMC- and XMC- compatible.

Memory resources include up to 16 GByte DDR4 SDRAM, 512 Kbit NVRAM and up to 256 GByte M.2 removable SATA Flash drive

Software choices include Built in Test (BIT) plus OS (64-bit only) support for Microsoft® Windows® 10, Linux® Fedora and Red Hat Linux, and VxWorks®.

1.2 Available Accessories

The following table lists the accessories that are available for the XVB603.

Table 1-1 Available Accessories

Item	Purpose
VTM29	Rear Transition Module, 6U x 4HE/HP
YLB-CR12-01	10-pin har-link® to COM Port Sub-D 9 pins adapter cable

1.3 Software Support

The XVB603 provides Intel Xeon processor with four cores with a shared memory and I/O resource pool. Customer system applications call for software platforms that support Symmetric Multiprocessing (SMP) operation as well as near real time support of independent application threads.

Generally, these different software needs require the support of multiple operating systems and require software driver and Board Support Packages (BSPs) to support the low-level hardware functions.

1.3.1 Device Driver Support

Standard Windows 10 video, chipset, and network drivers used for testing during development are available by contacting your Abaco representative. Standard Drivers for Linux should be available from the release OS vendor. Drivers for other specific XVB603 functions are available by purchasing the applicable OS Software Support Package from Abaco Systems.

1.3.2 UEFI Infrastructure Support

XVB603 uses Aptio UEFI that includes all functions required by the processor core and chipset. This package also includes the onboard hardware initialization code that is executed following release from reset.

The UEFI also provides ROM code that supports remote booting from any of the Ethernet ports.

1.3.3 Target Operating Systems

The XVB603 hardware supports Windows, Linux, and VxWorks operating systems.

Please contact local sales and support services for the most current operating system version information.

NOTE

The XVB603 is shipped with Compatibility Support Module (CSM) disabled in the CMOS setup. This allows the unit to operate in a UEFI-aware environment. Some operating systems may require special drive setup or parameters to use the UEFI mode. Contact your OS vendor for specifics needed for UEFI compatibility. If CSM Mode is needed for Legacy OS operation, it may be enabled in the advanced CMOS setup tab. See Section C.4.2 for CSM details.

1.4 Power Requirements

- +5V only
- ±12V for mezzanine only

1.5 Safety Notices

The following general safety precautions represent warnings of certain dangers of which Abaco Systems is aware. Failure to comply with these or with specific Warnings and/or Cautions elsewhere in this manual violates safety standards of design, manufacture and intended use of the equipment. Abaco Systems assumes no liability for the user's failure to comply with these requirements.

Also follow all warning instructions contained in associated system equipment manuals.

WARNING

Use extreme caution when handling, testing, and adjusting this equipment. This device may operate in an environment containing potentially dangerous voltages.

Ensure that all power to the system is removed before installing any device.

To minimize electric shock hazard, connect the equipment chassis and rack/enclosure to an electrical ground. If AC power is supplied to the rack/enclosure, the power jack and mating plug of the power cable must meet IEC safety standards.

1.5.1 Flammability

The XVB603 circuit board is made by a UL-recognized manufacturer and has a flammability rating of UL 94V-0.

1.5.2 EMI/EMC Regulatory Compliance

CAUTION

This equipment generates, uses, and can radiate electromagnetic energy. It may cause or be susceptible to EMI if not installed and used in a cabinet with adequate EMI protection.

The XVB603 is designed using good EMC practices and, when used in a suitably EMC-compliant chassis, should maintain the compliance of the total system.

The XVB603 is designed for use in systems meeting VDE class B, EN and FCC regulations for EMC emissions and susceptibility.

1.5.3 Handling

Only handle the XVB603 by the ejector handles or front panel.

1.5.4 Installation and Powerup/Reset

A Power button is located on the front panel and rear (via RTM). Please review the previous sections before installing the XVB603.

CAUTION

Ensure that the XVB603's power requirements are compatible with those supplied by the backplane. The XVB603 power requirements are up to 60+ W across the 5V and 12V rails. See Section A.9, "Electrical Characteristics".

2 • Unpacking and Installation

This chapter describes the installation of the XVB603 VME SBC on a VME backplane and initial power-on operations.

2.1 Unpacking Procedures

On receipt of the shipping container, check for any evidence of physical damage. All claims arising from shipping damage should be filed with the carrier and a complete report sent to Abaco Technical Support, see Technical Support Contact Information.

Electronic assemblies use devices that are sensitive to static discharge. Observe antistatic procedures when handling these boards. All products should be in an antistatic plastic bag or conductive foam for storage or shipment. Work at an approved antistatic workstation when unpacking boards.

2.2 Identifying Your Board

The board is identified by labels at strategic positions. These can be cross-checked against the Advice Note provided with your delivery.

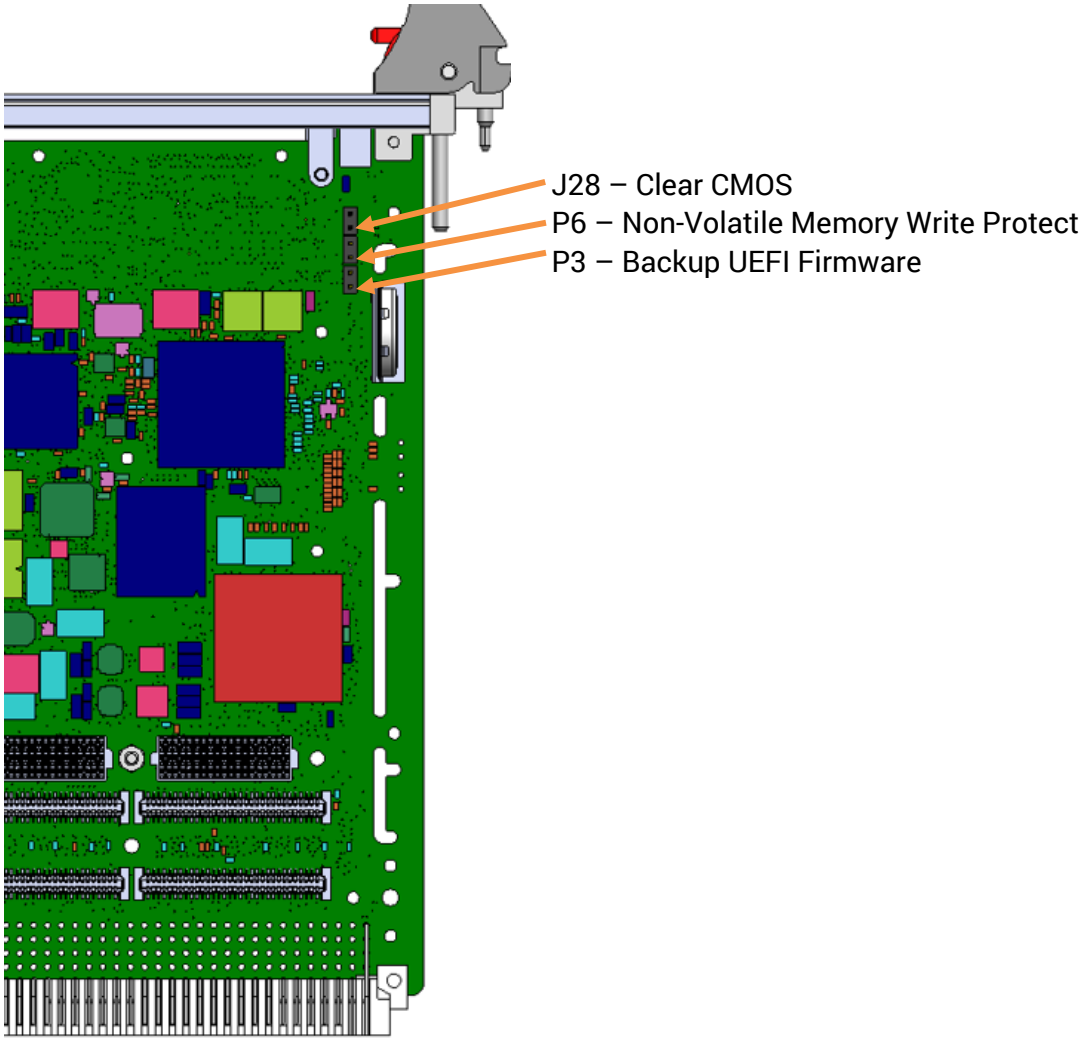
Identification labels attached to the shipping box and the antistatic bag give identical information: product code, product description and equipment number. On the board within the antistatic bag, there is an identifying label attached to the PCB.

2.3 Equipment Grounding

To minimize electric shock hazard, connect the equipment chassis and rack/enclosure to an electrical ground. If AC power is supplied to the rack/enclosure, the power jack and mating plug of the power cable must meet International Electrotechnical Commission (IEC) safety standards.

2.4 Jumper Headers

Figure 2-1 Jumper Header Locations



This manual refers to jumper settings as **In** or **Out**. Meanings are as follows:

In = jumper installed - 

Out = jumper not installed - 

NOTES

The XVB603 is shipped from the factory with no jumpers installed.

Ordinary operation requires no jumpers to be installed.

The state of the jumpers can be read from the FPGA Board Jumper Status Register (offset 0x6CD).

2.4.1 Clear CMOS Jumper Header (J28)

This header allows the user to clear the CMOS, which will reset all the settings in the UEFI to the factory defaults. See Section 3.3.1, "Clear CMOS/RTC/Password" for details.

Table 2-1 J28 Jumper Settings

Setting	Meaning
In	CMOS is cleared once power is applied
Out	CMOS is not affected (default)

2.4.2 NVRAM Write Enable Jumper Header (P6)

This header controls the write protection for the user NVRAM device on the XVB603 when NVRAM Write Protection in the UEFI is set to "NVMRO Controlled".

Table 2-2 P6 Jumper Settings

Setting	Meaning
In	Write Enabled
Out	Write Protected (default)

2.4.3 Backup UEFI Firmware Jumper Header (P3)

This header allows user selection of the SPI Flash device from which the XVB603 boots, as follows:

Table 2-3 P3 Jumper Settings

Setting	Meaning
In	XVB603 boots from backup device
Out	XVB603 boots from primary device (default)

The factory-programmed Backup device is for use if the Primary device is corrupted. In normal operation, this jumper is not installed, and the XVB603 boots from the Primary device.

Booting from the Backup device puts the XVB603 into Recovery mode.

2.5 Mezzanine Installation

The XVB603 has one mezzanine site that supports a compliant PMC or XMC. See Section D.1.2, “Mounting of PMC or XMC Module” for mounting instructions.

2.5.1 PMC Installation

The PMC site is factory-configurable to support either 3.3V or 5V VIO signaling voltage.

PMCs supplied by Abaco are delivered with a full kit of parts for mounting them. A PMC ordered with an XVB603 can be supplied factory-installed, if required.

CAUTION

Observe handling and antistatic precautions when installing the PMC.

It will usually be necessary to install driver software or implement other firmware configuration to achieve full functionality of a PMC (see the specific PMC manual for the exact procedure).

TIP

Where a PMC is not pre-installed, prove operation of the XVB603 *before* installing the PMC.

2.5.2 XMC Installation

XMCs supplied by Abaco are delivered with a full kit of parts for mounting them. Installing is similar to a PMC. An XMC ordered with an XVB603 can be supplied factory-installed, if required.

CAUTION

Observe handling and antistatic precautions when installing the XMC.

It will usually be necessary to install driver software or implement other firmware configuration to achieve full functionality of an XMC (see the specific XMC manual for the exact procedure).

TIP

Where an XMC is not pre-installed, prove operation of the XVB603 *before* installing the XMC.

2.6 Installation Preparation

Observe all safety procedures to avoid damaging the system and to protect operators and users. Use the following steps to install your Abaco hardware.

1. Ensure that the system power and external supplies have been turned off before installing or removing any board.
2. Check that the jumpers and mezzanine are correctly configured for your application.
3. Mount the board/mezzanine/transition module carefully. If applicable, see Section D.1.2, "Mounting of PMC or XMC Module".
4. Connect all I/O cables.
5. Restore the power once it is certain that all modules are correctly installed into the system, and all connections have been made properly.

2.6.1 VMEbus Products

On a standard VMEbus backplane, remove the jumpers on the IACKIN - IACKOUT interrupt daisy-chain (1 jumper) and on the BGxIN - BGxOUT bus grant daisy-chains (4 jumpers) for the slot where the board is to be mounted. The daisy-chain jumpers on the VMEbus backplane should be mounted on all free slots.

Setting jumpers is not necessary for the Abaco Auto-Daisy- Chain VMEbus backplane.

A board with system controller functionality must be installed into slot 1.

The backplane must supply +5V.

Because the board is available in several options, the description in this chapter is related to the standard configuration. Mount the CPU board carefully in the VME slot.

2.6.2 Replacing/Disposing of Batteries

There is danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by Abaco Systems.

Dispose of used batteries according to instructions of Abaco and applicable local regulations. See Section A.6, "Onboard Lithium Battery".

2.7 Required Items

The following items are required to start the XVB603 in a standard configuration.

2.7.1 Backplane and Power Supply

A standard VME backplane, wired into a regulated power supply capable of providing a stable low-noise +5V source, is required. Make sure that the supply can meet the total power requirements of the XVB603.

See Section A.9.1," Supply Voltage Range" for details.

Initially, you may plug the board into your 6U system slot of your VMEbus system. Make sure the power supply is OFF while plugging the board into the backplane.

2.7.2 Keyboard and Mouse

A compatible keyboard for initial system operation is required. Depending on the application, this keyboard may be a standard keyboard, or one which utilizes membrane switches for harsh environments. The keyboard is attached via a USB connector.

2.7.3 Video Monitor

The XVB603 offers front-panel access to the video signal through the DP (DisplayPort). Video is also available via the P2/P0 VME connector. To gain access to these pins, it is necessary to use the DVI-D connector on the transition module VTM29.

2.7.4 Minimum System Requirements

The XVB603 has been thoroughly tested and is ready for use in the target system. To verify XVB603 operation for the first time, it is suggested to configure a minimal system only. It is not necessary to have disk drives, a Flash disk or other accessories connected in order to perform the XVB603 Power-On Self-Test (POST). See Section 3.2, “POST” for details.

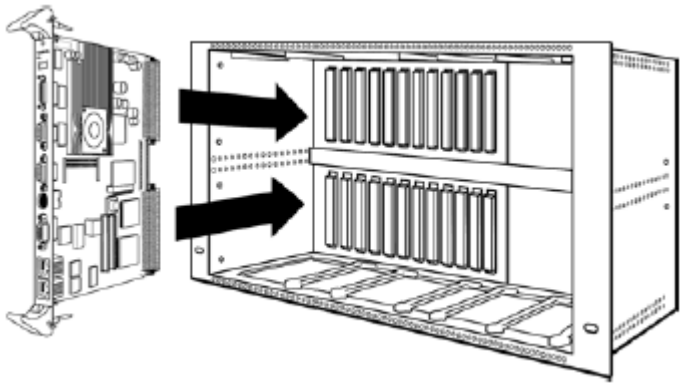
2.8 Installing XVB603 into Chassis

Boards are installed in a VME chassis by:

1. Sliding the board carefully into the guide rails
2. Inserting the board all the way until the handles can be operated to seat and lock the board in place. Handles typically have a lock (snap lever) to unlock them when extracting a board

Older boards may have screws instead of handles to secure the board in place.

Figure 2-2 6U Board Insertion into a Chassis



2.9 Connecting to the XVB603

To interact with onboard firmware requires the XVB603 to have, as a minimum, a terminal connection present on the serial COM3 port. Ethernet, video and USB connections may also be required, depending on Operating System requirements. These ports may be accessed either through the backplane pins, using a rear transition module or via the front I/O connectors.

COM3 is routed to the front panel with an RS-232 connection. COM1 and COM2 are 16550-compatible, full duplex, async serial ports and are routed to P2, accessible by the RTM (RS232/422/485). The ports feature independent 16-Byte FIFO, supporting baud rates up to 115k baud.

2.9.1 Front-Panel I/O

It is also possible to access COM3, Ethernet, DP video and USB ports along with optional SATA port through front-panel I/O connectors. See Section 4.2, “Front Panel Connectors” for details of each connection.

The following items are required:

- XVB603
- A serial 9-way adapter cable (contact your nearest sales office or agent)
- A null-modem 9-way D-type cable for connecting COM3 to a control terminal or PC running terminal emulation software

- For the Ethernet ports, a CAT5 (or better) straight-through patch cable for 10/100/1000BaseTX
- For video, a DVI or HDMI monitor with a DisplayPort, male 20-pin cable or adapter
- For USB 3.0 (backward compatible to USB 2.0), the required peripheral with a standard type A connector

CAUTION

Front Panel I/O cables should only be inserted or removed when power to the board is off, unless that I/O specification supports Hot Insertion removal. Inserting and removing the cable connectors of non-Hot Insertion/Removal I/O while the XVB603 is powered on may cause loss of data and result in system instability.

2.9.2 Rear Transition Module Installation

Connections to the Serial and Ethernet I/O can be achieved using the Rear Transition Module (RTM), which plugs into the XVB603 separated by the backplane.

The following items are required:

- XVB603
- VTM29 RTM
- A null-modem 9-way D to 9-way D-type cable for connecting COM1 and/or COM2 to a control terminal or PC running terminal emulation software
- For the Ethernet port, a CAT5 (or better) straight-through patch cable for 10/100/1000BaseTX
- For video, a DVI monitor with cable (DVI-D connection)
- For USB 2.0, the required peripheral with a standard type A connector
- USB keyboard and mouse are also supported

For more information on the VTM29 RTM, see the Hardware Reference Manual located at the following link.

CAUTION

Front Panel I/O cables should only be inserted or removed when power to the board is off, unless that I/O specification supports Hot Insertion removal. Inserting and removing the cable connectors of non-Hot Insertion/Removal I/O while the XVB603 is powered on may cause loss of data and result in system instability.

LINK

https://www.abaco.com/download/vtm29-hardware-reference-manual

2.10 Initial Powerup Operation

Once the required items are in place, the XVB603 is ready to be powered up. After a few seconds, the XVB603 system UEFI firmware banner will display on the screen. Display of all on-screen messages indicates the board is running properly and is ready to be installed and set up for application.

2.11 Entering the UEFI SETUP

To enter SETUP during the initial power-up sequence:

- Press the <ESC> or <DEL> key during the boot up sequence. Also see the applicable on-screen messages when prompted. See Appendix C, "UEFI Setup Utility" for a variety of menu options.

NOTE

Consult the User's Manual https://ami.com/ami_downloads/Aptio_TSE_Users_Guide.pdf for Aptio UEFI Firmware Setup for further general information on settings and configurations. This document is for **general reference only** and does not show specific XVB603 CMOS setup configurations.

If the board does not perform as described above, damage may have occurred in shipping or the board is not installed or setup properly. Contact Abaco Technical Support.

3 • Powerup/Booting

3.1 Power Supply

For exact power supply values, see Section A.5, “Power Consumption”. For rough data, a current of up to 10.8A at the 5V rail must be taken into consideration for a basic XVB603 powerup. (These are typical values and do not include backplane termination power or external drive power.) The XVB603 does not use ±12V, but they are provided to the PMC connectors for the mezzanine which uses these voltages. If there is a hard disk or PMC module attached to the XVB603, its power consumption must also be calculated.

Standard power supplies often require minimum loads on every supply voltage for proper operation. It may be necessary to add a load to the +12V to ensure correct voltage level on 5V.

If there are problems starting the board or doing resets at random states, check the voltage of the supply voltage at the backplane. Attach a standard digital multimeter to the backplane at positions where no high current is flowing.

It is advisable to use rear contacts of the bus connectors or unused power connectors for measuring. Measuring the voltage at the used power connectors can result in wrong values which are caused by the high current flowing.

The 5V should reach its nominal value when measuring with a multimeter. If the voltage is less than 5.0V when the CPU or memory perform intensively, the voltage may drop causing the XVB603 to reset.

3.2 POST

Each time the computer boots up it must pass the POST. The following is the procedure of the POST:

- The first step of POST is the testing of the Power Supply to ensure that it is turned on and that it releases its reset signal
- CPU must exit the reset status mode and thereafter be able to execute instructions
- UEFI is readable
- UEFI checksum must be valid, meaning that it must be readable
- CMOS RAM is readable
- CPU must be able to read all forms of memory such as the memory controller, memory bus, and memory module
- The first 1 MByte of memory must be operational and have the capability to be read and written to and from, and capable of containing the POST code
- I/O bus / controller must be accessible

If the computer passes all POST, then the UEFI video banner will be displayed on the applicable video device, and the board will attempt to boot to the default storage device.

Because the boards are available in several configurations, the description in this chapter is related to the standard configuration.

3.3 Setup

To enter the UEFI Firmware Setup, press the keyboard <ESC> or <DEL> key at the right moment. When using a slow starting monitor, it is advisable not to wait for the CRT to show the message 'Press either DEL or ESC to enter Setup'. When using add-on cards with external Option ROM's UEFI Firmware, press the DEL, F2 key while their program runs.

If the right moment was missed to press the <DEL> or <ESC> key, use the power button on the front panel to restart the powerup sequence or switch off the power supply for a few seconds and restart it.

Pressing the <F7> key will bring up Boot Device Selection window without having to go into Setup. See Section C.1, “Boot Device Selection Menu”.

3.3.1 Clear CMOS/RTC/Password

NOTE

The UEFI has the capability of password protecting casual access to the unit’s CMOS setup screens. Clearing the CMOS allows the user to clear the password in case of a forgotten password. This also clears all CMOS settings and restores factory defaults.

To clear the CMOS password:

1. Turn off power to the unit.
2. Remove the board from the chassis.
3. Install jumper onto header J28 (See Section 5.19, “Jumper Headers” for header location).
4. Insert board into chassis.
5. Turn on power to the unit and allow it to boot.
6. If the jumper can be accessed, it can be removed with power applied; otherwise, turn off power to the board, remove the board from the chassis and remove the jumper.

3.3.2 UEFI Setup

The XVB603 has an onboard UEFI Setup program that controls many configuration options. These options are saved in a special non-volatile memory area and are collectively referred to as the board's setup configuration. The setup configuration controls many details concerning the behavior of the hardware from the moment power is applied. To clear UEFI settings to factory defaults, refer to Section 3.3.1, "Clear CMOS/RTC/Password".

TIPS

It is recommended to ensure the board passes POST with default settings prior to changing the configuration.

Install a jumper on P6 prior to adjusting settings in the DIP Switch Configuration menu or the VMEbus Configuration menu of the BIOS. Once the changes have been made, reboot with the jumper installed. This will allow the newly adjusted settings to be activated. The jumper may be removed after powerup has completed.

Details of the XVB603 UEFI setup program are included in Appendix C, "UEFI Setup Utility".

NOTE

In this manual, the UEFI may also be referred to as BIOS.

CAUTION

Battery backup of critical CMOS settings is provided by the system via the VBAT signal on the VME backplane. If the board is removed from the backplane, these settings will be lost if no battery is installed onboard.

3.4 Unexpected Resets

A set of special registers is implemented onboard to locate the reset source in the event the XVB603 unexpectedly issues a reset and starts booting again. For every reset source set, there is a special bit that can be read in the next boot up.

See Table 7-9 and Table 7-10 for register details.

3.5 Remote Ethernet Booting

The XVB603 is capable of booting from a server using the 10/100/1000 Mbit Ethernet ports over a network utilizing the Intel Boot Agent. The Intel Boot Agent provides the ability to remotely boot the XVB603 using the PXE protocol. This feature allows users to create systems ensuring disk drive reliability, without the extra cost of adding NAND Flash drives.

4 • Connectors

This chapter describes the XVB603 front panel, onboard and backplane connectors and their pin assignments.

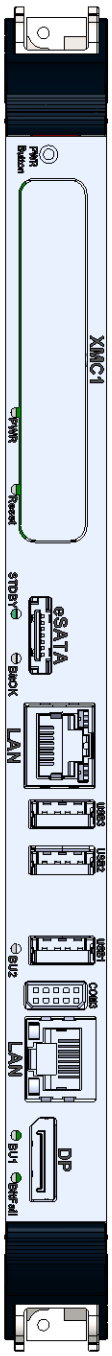
Table 4-1 Legend for PMC Tables

Notation	Meaning
#	Active Low Signal
N/C	Not Connected
RSVD	Do not connect anything (Reserved)
V(I/O)	I/O Voltage, connected with +3.3V

4.1 Front Panel Interface

Figure 4-1 shows the IEEE 1101.10 standard front panel with ejector handles (Contact the Abaco Sales Team for more details.). The I/O connectors are the same for both available front panel options.

Figure 4-1 Front Panel on XVB603 (IEEE 1101.10 Standard)



PWR – Power Good (Green LED)
Reset – Reset Status (Red LED)
STDBY – Standby Power from the backplane (Green LED)
BitOK – BIT Passed (Green LED)
BU2 – User-Programmable BIT Status #2 (Yellow LED)
BU1 – User Programmable BIT Status #1 (Yellow LED)
BitFail – BIT Failed (Red LED)

PMC1/XMC1

J9 eSATA

J3 GbE LAN RJ45

J27 USB 3.0

J2 USB 3.0

J1 USB 3.0

J7 Serial Port COM3

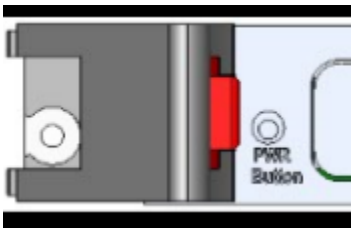
J8 GbE LAN RJ45

J5 Display Port

4.1.1 Power Button (S1)

There is a Power (PWR) Button on the front panel. An external Power Button may be connected between the appropriate I/O connector at the back side and ground (GND).

Figure 4-2 Power Button



With a short pressing at the PWR Button, the operating system tries to shut down the XVB603 to State S5. If the operating system does not react, a long pressing (>5 s) will shut down the XVB603 to State S5 without operating system support.

State S5 switches off the CPU core power and holds the XVB603 in reset. The state S5 is indicated by one of these two ways:

- Reset LED is ON and Power Good LED is OFF (front panel LEDs)
- Sleep Status LED is ON (bottom assembly LED)

See Section 5.18, "LEDs" for locations. At this state, it is possible to reactivate the XVB603 with a short press at the PWR Button. The CPU core voltage is switched on and the board restarts. This power off and power on cycle can be used to reset the XVB603.

4.2 Front Panel Connectors

The XVB603 Front Panel I/O is included in Levels 1 and 2 with the following interfaces:

- DisplayPort, 2x GbE, COM3, 3x USB 3.0, eSATA, PMC/XMC, Power Button
- LEDs: Power, Reset, STDBY, BitOK, 2x BIT Status/user-programmable, BitFail

  See Section 5.18.1, “Front I/O LEDs” for LED descriptions.

4.2.1 Front Panel DisplayPort (J5)

The front panel DisplayPort is one of the three graphic ports available on the XVB603. The front panel DisplayPort is a single, horizontal 20-pin connector that connects to an adapter/cable. For further information on the other video display types that are routed out the backplane, see Section 5.4, "Graphics Controller".

NOTE

Audio is not supported on the J5 DisplayPort connector.

Figure 4-3 DisplayPort Front Panel Connector (J5)

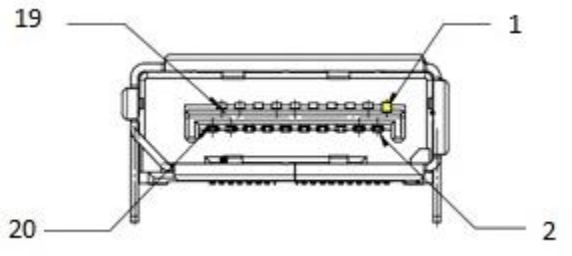


Table 4-2 DisplayPort (J5)

Pin	Signal	Pin	Signal
1	DPB_LANE0+	11	GND
2	GND	12	DPB_LANE3-
3	DPB_LANE0-	13	AUX_EN-
4	DPB_LANE1+	14	GND
5	GND	15	DPB_AUX+
6	DPB_LANE1-	16	GND
7	DPB_LANE2+	17	DPB_AUX-
8	GND	18	DPB_HPD
9	DPB_LANE2-	19	GND
10	DPB_LANE3+	20	3.3V

4.2.2 Front Panel Ethernet Interface RJ45 (J8 and J3)

The XVB603 has two Gigabit Ethernet (GbE) channels.

Figure 4-4 Ethernet RJ45 Interface

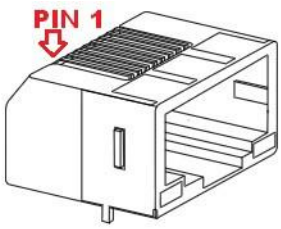


Table 4-3 LAN GbE (J8 and J3)

LAN	10/100BASE-T	1000BASE-T
1	TXD+	MDI0+
2	TXD-	MDI0-
3	RXD+	MDI1+
4	N/C	MDI2+
5	N/C	MDI2-
6	RXD-	MDI1-
7	N/C	MDI3+
8	N/C	MDI3-

Two LEDs (green and yellow) are integrated in each of the RJ45 connectors. These LEDs indicate the link status and activity of the interface.

Table 4-4 LEDs on LAN Connectors

LED	LED Status	Interface Status
1 (Green/Left)	On	Link
	Off	No Link
2 (Yellow/Right)	On, Blinking	TX/RX activity
	Off	No activity

4.2.3 Front Panel Serial Port COM3 (J7)

COM3 is accessible via the front panel connector and is RS232 only. A short custom har-link adapter cable is available to convert the 10-pin har-link connector to a standard Sub-D9 connector (Part No. YLB-CR12-01).

Figure 4-5 COM3 Location

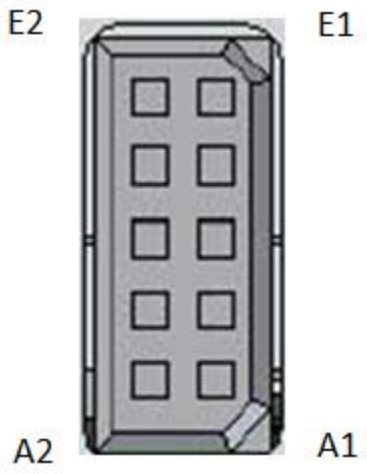


Table 4-5 Serial Port COM3 Connector (J7)

har-link Connector	RS232	DSUB Male Connector
A1	RXD	2
B1	TXD	3
C1	Reserved	N/A
D1	DTR	4
E1	DSR	6
A2	RTS	7
B2	RI*	9
C2	GND	5
D2	CTS	8
E2	DCD	1

* RI (Ring Indicator) is not supported on the XVB603.

4.2.4 Front Panel USB 3.0 Interface (J1, J2, J27)

The Front Panel USB 3.0 Standard A connectors are completely backward compatible with a USB 2.0 Standard A connector, with additional pins provided for USB 3.0 high speed differential signals.

Figure 4-6 USB 3.0 Interface

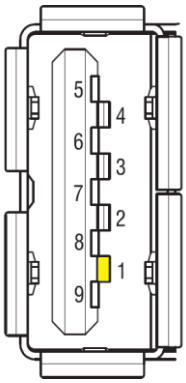


Table 4-6 USB 3.0 Connector Front Panel

Pin	Signal	Pin	Signal
1	VCC[1]	5	USB3.0_RX-
2	USB2.0-	6	USB3.0_RX+
3	USB2.0+	7	GND
4	GND	8	USB3.0_TX-
		9	USB3.0_TX+

[1]This pin is currently limited to 1.5A. For normal operation, do not exceed 1A current.

4.2.5 Front Panel eSATA Interface (J9)

The SATA port is capable of GEN 3 signaling but should be limited to GEN2 maximum speed when using eSATA cable lengths greater than 18 inches.

Figure 4-7 eSATA Front Panel Port (J9)

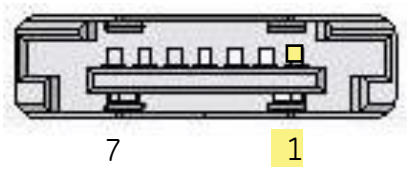
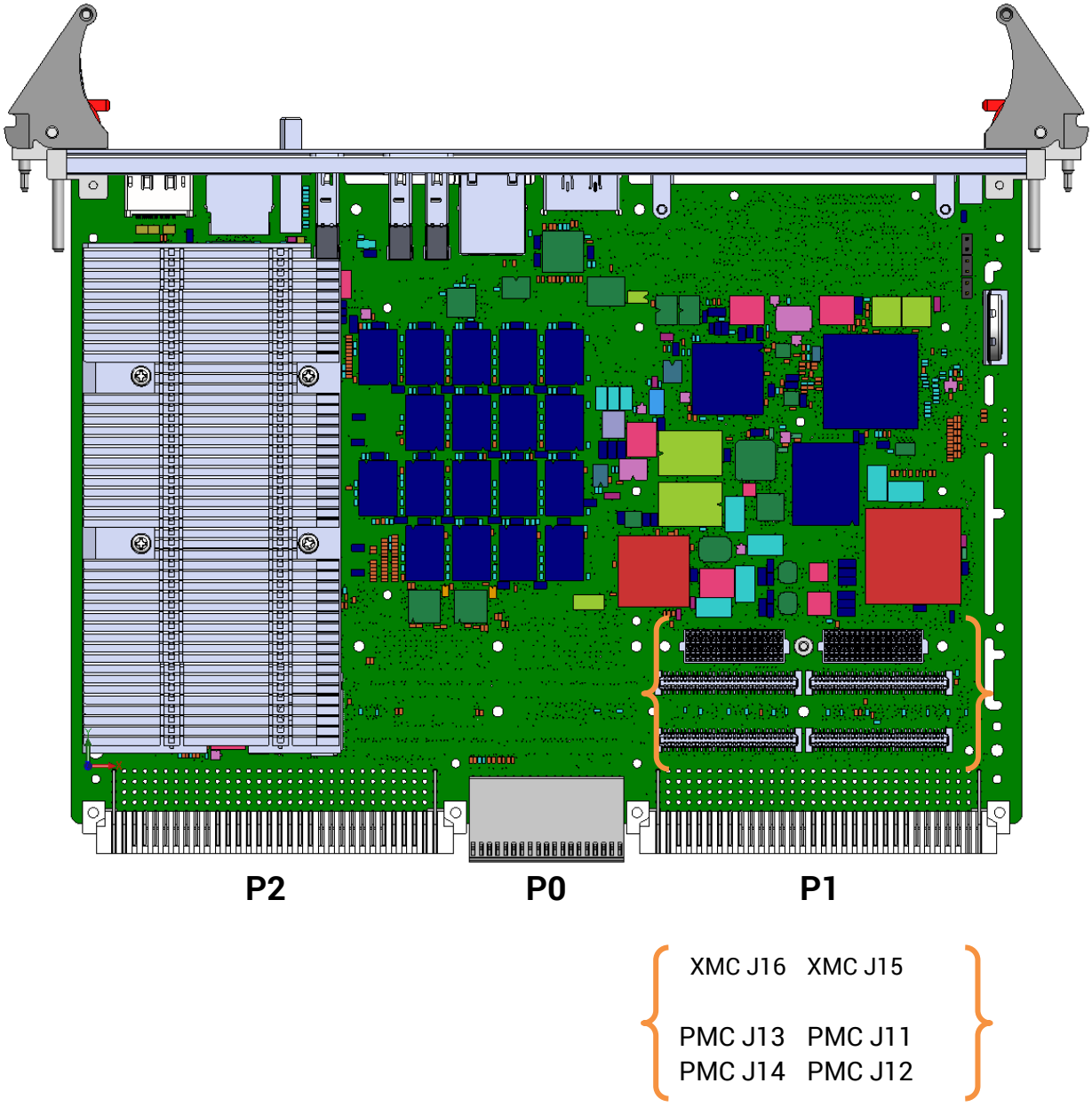


Table 4-7 SATAx/eSATA

Pin	Signal
2	SATA_TX+
3	SATA_TX-
5	SATA_RX-
6	SATA_RX+
1, 4, 7	GND

4.3 Onboard Connectors

Figure 4-8 XVB603 Top Assembly View of Levels 1 and 2



4.3.1 PMC I/O Options

There are specific versions of PMC plug-on modules which require specific pin assignments on the VME connectors to be able to use the PMC I/O options and to avoid damage to the XVB603. See Appendix D, "Mezzanine Site".

4.3.2 PMC Connectors (J11, J12, J13)

The following tables list the pin assignments of the onboard PMC connectors (J11, J12). The PMC slot is 64-bit, up to PCI-X 133 MHz capable and works with a PCIe-PCI bridge (Pericom PI7C9X130). The PCI bridge and PMC-bus are disabled when a PMC card is not installed or an XMC card is installed at this slot. The PCI Signaling voltage is fixed at +3.3V. (See the UEFI Development PC Setup User Manual at www.ami.com).

The PMC is electrically and mechanically compliant to specification IEEE 1386 and 1386.1 with enhancements of the Processor PMC Standard VITA 32-2003. These enhancements provide pins for a secondary agent; (IDSELB and REQB / GNTB) but do not support a monarch PMC card.

Figure 4-9 PMC Connector Pin Assignments (J11)

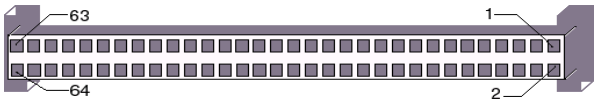


Table 4-8 PMC Connector Pin Assignments (J11)

Signal	Pin	Pin	Signal
TCK*	01	02	-12V
GND	03	04	PMCINTA#
PMCINTB#	05	06	PMCINTC#
PRESENT#	07	08	+5V
PMCINTD#	09	10	RSVD
GND	11	12	RSVD
PCICLK	13	14	GND
GND	15	16	GNT0#
REQ0#	17	18	+5V
V(I/O)	19	20	AD31
AD28	21	22	AD27
AD25	23	24	GND
GND	25	26	CBE[3]#
AD22	27	28	AD21
AD19	29	30	+5V
V(I/O)	31	32	AD17
FRAME#	33	34	GND
GND	35	36	IRDY#
DEVSEL#	37	38	+5V
PCIXCAP	39	40	LOCK#
SDONE	41	42	SBO#
PAR	43	44	GND
V(I/O)	45	46	AD15
AD12	47	48	AD11
AD9	49	50	+5V
GND	51	52	CBE[0]#
AD6	53	54	AD5
AD4	55	56	GND
V(I/O)	57	58	AD3
AD2	59	60	AD1
AD0	61	62	+5V
GND	63	64	REQ64#

* This signal is specific to JTAG and reserved for factory use only.

Figure 4-10 PMC Connector Pin Assignments (J12)

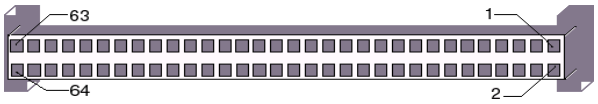


Table 4-9 PMC Connector Pin Assignments (J12)

Signal	Pin	Pin	Signal
+12V	01	02	TRST#[b]
TMS[b]	03	04	TDO[b]
TDI[b]	05	06	GND
GND	07	08	RSVD
RSVD	09	10	RSVD
PUP#[a]	11	12	+3.3V
PCIRST#	13	14	PDN1#[a]
+3.3V	15	16	PDN2#[a]
PME#	17	18	GND
AD30	19	20	AD29
GND	21	22	AD26
AD24	23	24	+3.3V
IDSEL	25	26	AD23
+3.3V	27	28	AD20
AD18	29	30	GND
AD16	31	32	CBE[2]#
GND	33	34	IDSELB#
TRDY#	35	36	+3.3V
GND	37	38	STOP#
PERR#	39	40	GND
+3.3V	41	42	SERR#
CBE[1]#	43	44	GND
AD14	45	46	AD13
M66EN	47	48	AD10
AD8	49	50	+3.3V
AD7	51	52	REQB#
+3.3V	53	54	GNTB#
RSVD	55	56	GND
RSVD	57	58	N/C
GND	59	60	PPMCRST#
ACK64#	61	62	+3.3V
GND	63	64	N/C

[a] Weak (330R) pull-down (PDN) to GND or 4.7k pull-up (PUP) to VIO.
[b] These signals are specific to JTAG and reserved for factory use only.

Figure 4-11 PMC Connector Pin Assignments (J13)

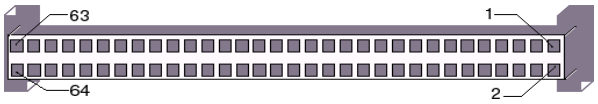


Table 4-10 PMC Connector Pin Assignments (J13)

Signal	Pin	Pin	Signal
RSVD	01	02	GND
GND	03	04	CBE[7]#
CBE[6]#	05	06	CBE[5]#
CBE[4]#	07	08	GND
V(I/O)	09	10	PAR64
AD63	11	12	AD62
AD61	13	14	GND
GND	15	16	AD60
AD59	17	18	AD58
AD57	19	20	GND
V(I/O)	21	22	AD56
AD55	23	24	AD54
AD53	25	26	GND
GND	27	28	AD52
AD51	29	30	AD50
AD49	31	32	GND
GND	33	34	AD48
AD47	35	36	AD46
AD45	37	38	GND
V(I/O)	39	40	AD44
AD43	41	42	AD42
AD41	43	44	GND
GND	45	46	AD40
AD39	47	48	AD38
AD37	49	50	GND
GND	51	52	AD36
AD35	53	54	AD34
AD33	55	56	GND
V(I/O)	57	58	AD32
RSVD	59	60	RSVD
RSVD	61	62	GND
GND	63	64	RSVD

4.3.3 PMC I/O Connector (J14)

PMC I/O signals are daisy chained between XMC connector J16, PMC connector J14 and the VME P2 connector.

Figure 4-12 PMC Connector Pin Assignments (J14)

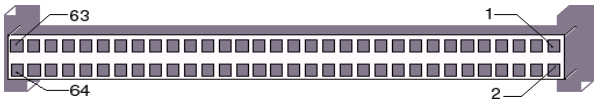


Table 4-11 PMC I/O Connector Pin Assignments (J14)

Signal	Pin	Pin	Signal
XMC_PMC_01	1	2	XMC_PMC_02
XMC_PMC_03	3	4	XMC_PMC_04
XMC_PMC_05	5	6	XMC_PMC_06
XMC_PMC_07	7	8	XMC_PMC_08
XMC_PMC_09	9	10	XMC_PMC_10
XMC_PMC_11	11	12	XMC_PMC_12
XMC_PMC_13	13	14	XMC_PMC_14
XMC_PMC_15	15	16	XMC_PMC_16
XMC_PMC_17	17	18	XMC_PMC_18
XMC_PMC_19	19	20	XMC_PMC_20
XMC_PMC_21	21	22	XMC_PMC_22
XMC_PMC_23	23	24	XMC_PMC_24
XMC_PMC_25	25	26	XMC_PMC_26
XMC_PMC_27	27	28	XMC_PMC_28
XMC_PMC_29	29	30	XMC_PMC_30
XMC_PMC_31	31	32	XMC_PMC_32
XMC_PMC_33	33	34	XMC_PMC_34
XMC_PMC_35	35	36	XMC_PMC_36
XMC_PMC_37	37	38	XMC_PMC_38
XMC_PMC_39	39	40	XMC_PMC_40
XMC_PMC_41	41	42	XMC_PMC_42
XMC_PMC_43	43	44	XMC_PMC_44
XMC_PMC_45	45	46	XMC_PMC_46
XMC_PMC_47	47	48	XMC_PMC_48
XMC_PMC_49	49	50	XMC_PMC_50
XMC_PMC_51	51	52	XMC_PMC_52
XMC_PMC_53	53	54	XMC_PMC_54
XMC_PMC_55	55	56	XMC_PMC_56
XMC_PMC_57	57	58	XMC_PMC_58
XMC_PMC_59	59	60	XMC_PMC_60
XMC_PMC_61	61	62	XMC_PMC_62
XMC_PMC_63	63	64	XMC_PMC_64

4.3.4 XMC Connector (J15)

The following tables list the pin assignments of the onboard XMC connectors. The XMC slot provides an x8 lane wide PCI Express interface. Only if an XMC mezzanine board is installed are the PCI express lanes connected to the XMC slot; otherwise, these lanes are connected to the PMC bridge.

The XMC Connectors J15 and J16 are electrically and mechanically compliant to the specification VITA 42.0 and IEEE 1386.1.

Figure 4-13 XMC Connector J15 and J16

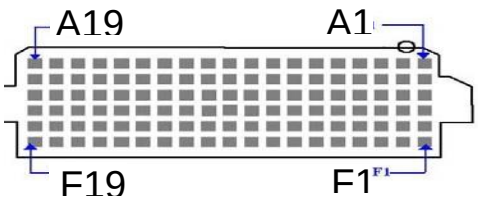


Table 4-12 XMC Connector Pin Assignments (J15)

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	RX0+	RX0-	+3.3V	RX1+	RX1-	+5V
2	GND	GND	TRST#[c]	GND	GND	XMCRSTIN#[a]
3	RX2+	RX2-	+3.3V	RX3+	RX3-	+5V
4	GND	GND	TCK[c]	GND	GND	XMC_RSTOUT#[b]
5	RX4+	RX4-	+3.3V	RX5+	RX5-	+5V
6	GND	GND	TMS[c]	GND	GND	+12V
7	RX6+	RX6-	+3.3V	RX7+	RX7-	+5V
8	GND	GND	TDI[c]	GND	GND	-12V
9	N/C	N/C	RPS	N/C	N/C	+5V
10	GND	GND	TDO[c]	GND	GND	GA0/GND
11	TX0+	TX0-	MBIST#	TX1+	TX1-	+5V
12	GND	GND	GA1/GND	GND	GND	XMCPRESENT#
13	TX2+	TX2-	+3.3V AUX	TX3+	TX3-	+5V
14	GND	GND	GA2/GND	GND	GND	BMC_SDA
15	TX4+	TX4-	RPS	TX5+	TX5-	+5V
16	GND	GND	MVMRO	GND	GND	BMC_SCL
17	TX6+	TX6-	N/C	TX7+	TX7-	N/C
18	GND	GND	N/C	GND	GND	N/C
19	CLK+	CLK-	N/C	N/C	N/C	N/C

[a] Reset driven by XVB603
[b] Reset driven by Mezzanine
[c] These signals are specific to JTAG and reserved for factory use only.

NOTE

For the XVB603 with the expansion board option, the J15 connector acts as the bridge connecting the EXP238 expansion board to the XVB603 and is not available for XMC use. While the J15 has the same pinout for this option of the XVB603, the height of the connector is larger than the standard XMC connector.

4.3.5 XMC Connector (J16)

XMC I/O are daisy chained between XMC connector J16, PMC connector J14 and the VME P2 connector.

Table 4-13 XMC Connector Pin Assignments (J16)

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	XMC_PMC_19	XMC_PMC_20	N/C	XMC_PMC_17	XMC_PMC_18	N/C
2	GND	GND	N/C	GND	GND	N/C
3	XMC_PMC_23	XMC_PMC_24	N/C	XMC_PMC_21	XMC_PMC_22	N/C
4	GND	GND	N/C	GND	GND	N/C
5	XMC_PMC_29	XMC_PMC_30	N/C	XMC_PMC_27	XMC_PMC_28	N/C
6	GND	GND	N/C	GND	GND	N/C
7	XMC_PMC_33	XMC_PMC_34	N/C	XMC_PMC_31	XMC_PMC_32	N/C
8	GND	GND	XMC_PMC_01	GND	GND	XMC_PMC_02
9	XMC_PMC_39	XMC_PMC_40	XMC_PMC_03	XMC_PMC_37	XMC_PMC_38	XMC_PMC_04
10	GND	GND	XMC_PMC_05	GND	GND	XMC_PMC_06
11	XMC_PMC_43	XMC_PMC_44	XMC_PMC_07	XMC_PMC_41	XMC_PMC_42	XMC_PMC_08
12	GND	GND	XMC_PMC_09	GND	GND	XMC_PMC_10
13	XMC_PMC_49	XMC_PMC_50	XMC_PMC_11	XMC_PMC_47	XMC_PMC_48	XMC_PMC_12
14	GND	GND	XMC_PMC_13	GND	GND	XMC_PMC_14
15	XMC_PMC_53	XMC_PMC_54	XMC_PMC_15	XMC_PMC_51	XMC_PMC_52	XMC_PMC_16
16	GND	GND	XMC_PMC_25	GND	GND	XMC_PMC_26
17	XMC_PMC_59	XMC_PMC_60	XMC_PMC_35	XMC_PMC_57	XMC_PMC_58	XMC_PMC_36
18	GND	GND	XMC_PMC_45	GND	GND	XMC_PMC_46
19	XMC_PMC_63	XMC_PMC_64	XMC_PMC_55	XMC_PMC_61	XMC_PMC_62	XMC_PMC_56

	GA2	GA1	GA0
XMC	0	0	0

4.4 Backplane Connectors

4.4.1 VMEbus Connector (P0 - Optional)

The VME P0 connector load is optional. When loaded, the P0 connector supplies two Gigabit Ethernet ports, Limited PMC I/O, DVI2 Port, and Two SATA ports as shown below:

Table 4-14 VMEbus Connector P0 with Partial PMC I/O

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	GND	GND	GND	GND	GND	GND
2	ETH3_0+	ETH3_0-	GND	ETH3_2+	ETH3_2-	GND
3	ETH3_1+	ETH3_1-	GND	ETH3_3+	ETH3_3-	GND
4	ETH4_0+	ETH4_0-	GND	ETH4_2+	ETH4_2-	GND
5	ETH4_1+	ETH4_1-	GND	ETH4_3+	ETH4_3-	GND
6	ETH3_LED_ACT#	ETH4_LED_ACT#	3.3V (RTM Power)	ETH3_LED_LINK#	ETH4_LED_LINK#	GND
7	RSVD	RSVD	RSVD	RSVD	RSVD	GND
8	RSVD	RSVD	RSVD	RSVD	RSVD	GND
9	RSVD	RSVD	RSVD	RSVD	RSVD	GND
10	RSVD	RSVD	RSVD	RSVD	RSVD	GND
11	RSVD	RSVD	RSVD	RSVD	RSVD	GND
12	RSVD	RSVD	RSVD	RSVD	RSVD	GND
13	RSVD	RSVD	RSVD	RSVD	RSVD	GND
14	RSVD	RSVD	RSVD	RSVD	RSVD	GND
15	RSVD	RSVD	RSVD	RSVD	RSVD	GND
16	DVI2TXC-	DVI2TXC+	SATA4RX+	SATA4RX-	RSVD	GND
17	DVI2TX0-	DVI2TX0+	DVI2HPD	SATA4TX+	SATA4TX-	GND
18	DVI2TX1-	DVI2TX1+	DVI2_SCL	SATA3RX+	SATA3RX-	GND
19	DVI2TX2-	DVI2TX2+	DVI2_SDA	SATA3TX+	SATA3TX-	GND

NOTES

The LAN pin assignment is compliant to the VITA 31.1 specification Gigabit Ethernet on VME64x Backplanes.

Ethernet port numbering adheres to the Intel chipset signal and board UEFI/EFI numbering.

Ethernet	Reserved (RSVD)	GND
DVI2	SATA	Power

4.4.2 VMEbus Connector (P1)

The following table lists the pin assignments of connector P1. The connector is compatible to the P1 connector of the VMEbus specifications ANSI/VITA 1 (VME64), ANSI/VITA 1.1 (VME64x), and VITA 38 (System Management).

Table 4-15 VMEbus Connector P1

Pin	Row Z	Row A	Row B	Row C	Row D
1	TRST#*	VMED00	VMEBBSY#	VMED08	+5V
2	GND	VMED01	VMEBCLR#	VMED09	GND
3	TCK*	VMED02	VMEACFAIL#	VMED10	RSVD
4	GND	VMED03	VMEBG0IN#	VMED11	RSVD
5	TDO*	VMED04	VMEBG0OUT#	VMED12	RSVD
6	GND	VMED05	VMEBG1IN#	VMED13	RSVD
7	TDI*	VMED06	VMEBG1OUT#	VMED14	RSVD
8	GND	VMED07	VMEBG2IN#	VMED15	RSVD
9	TMS*	GND	VMEBG2OUT#	GND	GAP#
10	GND	VMESYSCLK	VMEBG3IN#	VMESYSFAIL#	GA0#
11	RSVD	GND	VMEBG3OUT#	VMEBERR#	GA1#
12	GND	VMEDS1#	VMEBR0#	VMESYSRESET#	+3.3V (Not Used)
13	RSVD	VMEDS0#	VMEBR1#	VMELWORD#	GA2
14	GND	VMEWRITE#	VMEBR2#	VMEAM5	+3.3V (Not Used)
15	RSVD	GND	VMEBR3#	VMEA23	GA3
16	GND	VMEDTACK#	VMEAM0	VMEA22	+3.3V (Not Used)
17	RSVD	GND	VMEAM1	VMEA21	GA4
18	GND	VMEAS#	VMEAM2	VMEA20	+3.3V (Not Used)
19	RSVD	GND	VMEAM3	VMEA19	SMB_SCL
20	GND	VMEIACK#	GND	VMEA18	+3.3V (Not Used)
21	RSVD	VMEIACKIN#	IPMB_SCL	VMEA17	SMB_SDA
22	GND	VMEIACKOUT#	IPMB_SDA	VMEA16	+3.3V (Not Used)
23	RSVD	VMEAM4	GND	VMEA15	SMB_ALERT
24	GND	VMEA07	VMEIRQ7#	VMEA14	+3.3V (Not Used)
25	RSVD	VMEA06	VMEIRQ6#	VMEA13	RSVD
26	GND	VMEA05	VMEIRQ5#	VMEA12	+3.3V (Not Used)
27	RSVD	VMEA04	VMEIRQ4#	VMEA11	RSVD
28	GND	VMEA03	VMEIRQ3#	VMEA10	+3.3V (Not Used)
29	RSVD	VMEA02	VMEIRQ2#	VMEA09	RSVD
30	GND	VMEA01	VMEIRQ1#	VMEA08	+3.3V (Not Used)
31	RSVD	-12V	+5V STDBY	+12V	GND
32	GND	+5V	+5V	+5V	+5V

* These signals are specific to JTAG and reserved for factory use only.

4.4.3 VMEbus Connector (P2)

The following table lists the pin assignments of connector P2. Row B of the connector is compatible to connector P2 of the VMEbus specifications ANSI/VITA 1 (VME64) and ANSI/VITA 1.1 (VME64x).

Rows A and C are compliant to the VMEbus specifications ANSI/VITA 1 (VME64) and ANSI/VITA 1.1 (VME64x), ANSI/VITA 35-2000 chapter 2.3 ´Mapping of Single PMC-P4 to VME-P2 Rows A, C´.

Table 4-16 VMEbus Connector P2

Pin	Row Z	Row A	Row B	Row C	Row D
1	USB2_4+	XMC_PMC_02	+5V	XMC_PMC_01	DVI1TXC+
2	GND	XMC_PMC_04	GND	XMC_PMC_03	DVI1TXC-
3	USB2_4-	XMC_PMC_06	RETRY#	XMC_PMC_05	DVI1TX0+
4	GND	XMC_PMC_08	VMEA24	XMC_PMC_07	DVI1TX0-
5	USB2_5+	XMC_PMC_10	VMEA25	XMC_PMC_09	DVI1TX1+
6	GND	XMC_PMC_12	VMEA26	XMC_PMC_11	DVI1TX1-
7	USB2_5-	XMC_PMC_14	VMEA27	XMC_PMC_13	DVI1TX2+
8	GND	XMC_PMC_16	VMEA28	XMC_PMC_15	DVI1TX2-
9	HW_WP	XMC_PMC_18	VMEA29	XMC_PMC_17	DVI1HPD
10	GND	XMC_PMC_20	VMEA30	XMC_PMC_19	PWR_BTN_IN#
11	OC2_USB#	XMC_PMC_22	VMEA31	XMC_PMC_21	CODEC_PCBEEP
12	GND	XMC_PMC_24	GND	XMC_PMC_23	DDCC_DVI1
13	RST_LED#	XMC_PMC_26	+5V	XMC_PMC_25	DDCD_DVI1
14	GND	XMC_PMC_28	VMED16	XMC_PMC_27	SATA2RX+
15	BMC_BITFAIL#	XMC_PMC_30	VMED17	XMC_PMC_29	SATA2RX-
16	GND	XMC_PMC_32	VMED18	XMC_PMC_31	GPIO1
17	GPIO0	XMC_PMC_34	VMED19	XMC_PMC_33	C1_RXD
18	GND	XMC_PMC_36	VMED20	XMC_PMC_35	C1_RTS
19	SATA1TX+	XMC_PMC_38	VMED21	XMC_PMC_37	C1_TXD
20	GND	XMC_PMC_40	VMED22	XMC_PMC_39	C1_CTS
21	SATA1TX-	XMC_PMC_42	VMED23	XMC_PMC_41	GPIO2
22	GND	XMC_PMC_44	GND	XMC_PMC_43	GPIO3
23	SATA1RX+	XMC_PMC_46	VMED24	XMC_PMC_45	GPIO4
24	GND	XMC_PMC_48	VMED25	XMC_PMC_47	GPIO5
25	SATA1RX-	XMC_PMC_50	VMED26	XMC_PMC_49	C2_RXD
26	GND	XMC_PMC_52	VMED27	XMC_PMC_51	C2_RTS
27	SATA2TX+	XMC_PMC_54	VMED28	XMC_PMC_53	C2_TXD
28	GND	XMC_PMC_56	VMED29	XMC_PMC_55	C2_CTS
29	SATA2TX-	XMC_PMC_58	VMED30	XMC_PMC_57	GPIO6
30	GND	XMC_PMC_60	VMED31	XMC_PMC_59	GPIO7
31	3.3V	XMC_PMC_62	GND	XMC_PMC_61	GND
32	GND	XMC_PMC_64	+5V	XMC_PMC_63	+5V

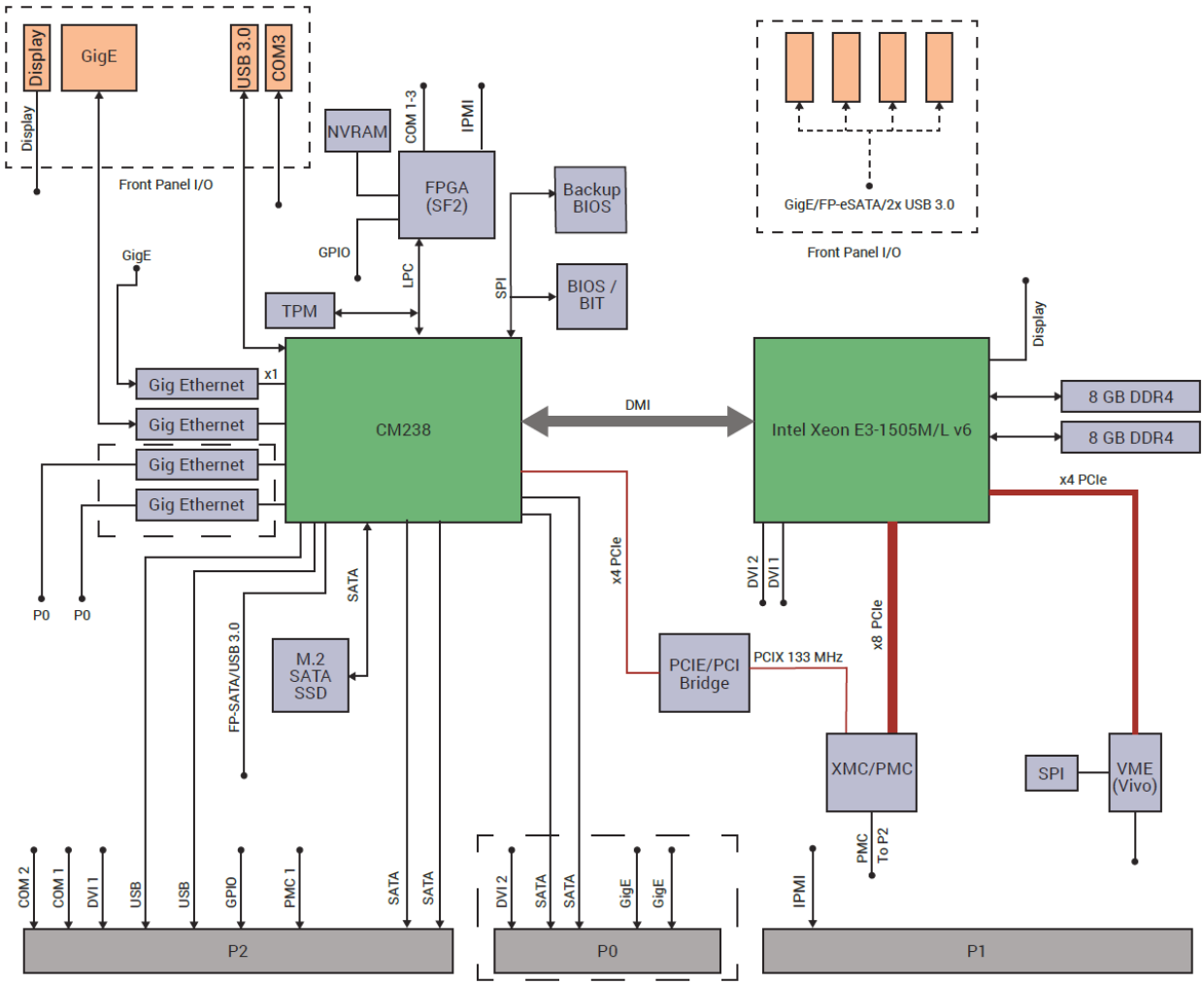
5 • Functional Description

This chapter describes the functions of the XVB603 built on Intel's architecture of the Operating Platform consisting of the Xeon Processor and the Mobile Intel CM238 Chipset.

The Xeon processor family provides an integrated memory hub and 2D/3D graphics controller. Enhanced Intel Turbo Boost® technology provides the ability to adjust the power and performance of the processor based on CPU and graphic demand.

The processor die is thermally protected by two thermal monitor features. When reaching a maximum safe operating temperature, the Thermal Control Circuit in the processor activates a frequency reducing feature and reduces the voltage and frequency dynamically. In case of a catastrophic die overheating (above 125 °C), the XVB603 switches off the processor core voltage. Recovery from this catastrophic event can be accomplished with a power off-on cycle or Power Button.

Figure 5-1 Block Diagram



5.1 Xeon 1505M v6 Intel Quad Core Processor

5.1.1 Xeon Processor Features

- Four execution cores
- Xeon 1505M v6 (Quad Core) @ 3.0 GHz (45W) base frequency or XEON 1505L v6 (QUAD Core LP) @ 2.2 GHz (25 W) base frequency (See Appendix E, "Processor Speed and Temperature")
- BGA Exact SKUs 4C GT2 45W/25W cTDP to 35W
- 8 MBytes shared cache
- Up to one x16, two x8 or one x8 + two x4 PCIe Gen 3 interfaces
- Dynamic DDR4 Memory
- Dual 64-bit memory controllers with ECC and SPD, DDR4, 2400 MHz (operating at 2133 MHz) (See Section 5.3, "CPU Memory Controller")
- Internal 3D Graphics processor

NOTE

PCIe ports are capable of supporting Gen1, Gen2 and Gen3; however, the ports are defaulted to Gen2 to allow compatibility to onboard and add-on devices.

5.1.2 Processor Supported Technologies

- Graphics support for DirectX® 12, OpenCL™ 2.0, OpenGL® 4.4
- Intel Hyper-Threading Technology (Intel HT Technology) two threads per core
- Intel 64 architecture
- Intel Turbo Boost Technology
- Intel Advanced Vector Extensions (AVX 2.0 extensions)
- Advanced Encryption Standard New Instructions (AES-NI)

5.1.3 Processor to PCH

- Direct Media Interface (DMI) connects the processor and Peripheral Controller Hub (PCH)

5.2 CM238 Chipset

Intel's CM238 Chipset supports the CPU and provides extensive I/O support for the XVB603. This includes:

- Eight PCI Express ports from the CM238 Chipset; Three ports from the CPU (See Section 5.5, "PCI Express Interfaces")
- ACPI Power Management Logic, Revision 4.0a
- Enhanced Direct Memory Access (DMA) controller, interrupt controller, and timer functions
- Integrated Serial ATA host controllers
    - with independent DMA
    - operation of up to six ports
- USB host interface
    - XHCI Host Controllers supporting SuperSpeed USB 3.0 (front I/O)
- System Management Bus (SMBus) interface
- Supports Intel Rapid Storage Technology
- Supports Intel Virtualization Technology for Directed I/O
- Three digital ports are supported in the CPU
    - DisplayPort (Front Panel)
    - Two DVI ports (Rear I/O)
- Serial Peripheral Interface (SPI) support
- Support for TXT (Trusted Execution Technology)

5.3 CPU Memory Controller

The CPU integrated dual-channel memory controller in the XVB603 supports dual data rate synchronous DRAM (DDR4) with a data bus width of 64 bits. The XVB603 offers 8 GBytes or 16 GBytes of SDRAM with full ECC support.

CAUTION

Caution must be used when sharing memory between the local processor and the VME to prevent a VME deadlock and to prevent a VME master from overwriting the local processor's operating system.

5.3.1 Memory Controller Features

- Dynamic DDR4 Memory
  - Memory DDR4 data transfer rates of 2133 MT/s
- Dual 64-bit memory controllers with ECC and SPD, DDR4, 2133 MHz
  - 8 GByte and 16 GByte options
- Unbuffered DDR4
- Theoretical maximum memory bandwidth of 21.3 GByte/s in dual channel mode assuming DDR4 2133 MT/s
- Intel Fast Memory Access
  - Just-in-time Command Scheduling
  - Command overlap
  - Out-of-order scheduling

5.4 Graphics Controller

The XVB603 uses integrated 2D/3D Graphics in the Intel Xeon Mobile processor and PCH, supporting analog and digital display ports. XVB603 HD Graphics P630 support for DirectX 12, OpenCL 2.0, OpenGL 4.4 and are integrated into the processor through the following five interfaces:

- One front panel DisplayPort (DP) (Audio is not supported on this DisplayPort connector)
- Two DVI ports (via Rear P2 and P0)

NOTE

DX, OpenCL and OpenGL support may vary based on platform configuration.

- DVI-1, when chosen as an option, is connected to DisplayPort C of the PCH. The maximum pixel rate is 165 MHz at 1920x1200. The port is connected to rear P2.
- DVI-2, when chosen as an option, is connected to DisplayPort D of the PCH. The maximum pixel rate is 165 MHz at 1920x1200. The port is connected to rear P0.

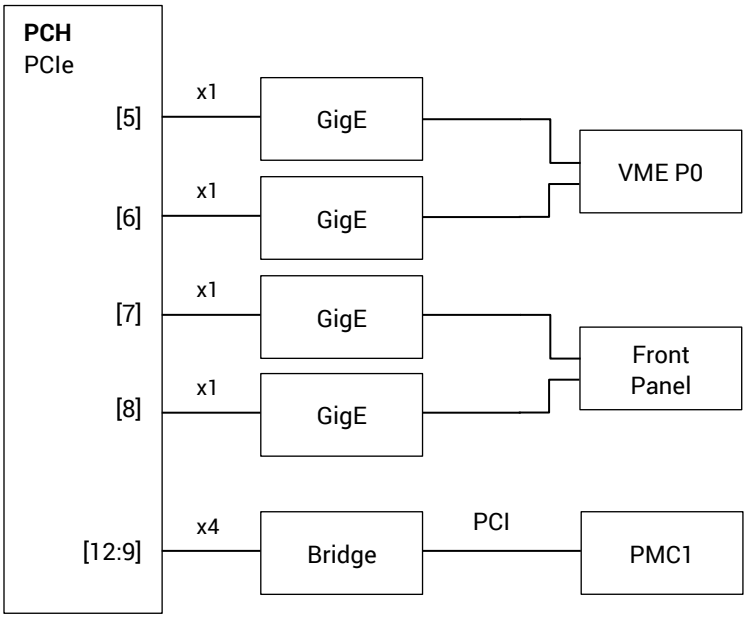
At higher resolutions, the cable and connectors have a greater influence on picture quality. Using high quality cables and connectors or reducing resolution enhances display.

5.5 PCI Express Interfaces

The Intel Xeon CPU and Intel PCH offer several PCI Express interfaces. The PCI Express channels are dedicated to the following devices:

5.5.1 CM238 Chipset Root Complex

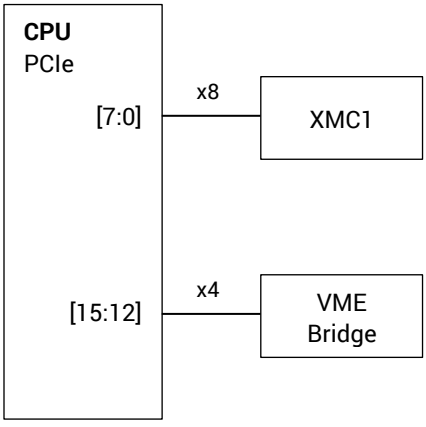
Figure 5-2 PCI Express Channels



5.5.2 Xeon CPU Root Complex

- x8 PCIe port connects to XMC site 1
- x4 PCIe port to VME bridge

Figure 5-3 CPU Root Complex



5.6 Mezzanine PMC/XMC Interface

The PCI Mezzanine Card (PMC) or XMC interface creates additional slots for parallel mounted expanders or option cards. The PCI bus for the PMC's site is provided by a Pericom PI7c9x130 PCIe to PCI bridges and has a 64-bit wide bus with PCI-X 133 MHz capability. If no PMC or XMC module is installed, the bridge is disabled and not visible on the PCI bus. If an XMC mezzanine card is mounted at the slot, the PCIe bus is provided by a x8 connection to the CPU root complex. See Appendix D, "Mezzanine Site".

5.7 VME Interface

The PCIe Root Complex for the VME interface is the Intel Xeon CPU. The VME interface is provided with the FPGA-based VME controller. It contains a complete high-performance 64-bit 2eSST-capable VMEbus interface. A system controller is implemented in the VME Controller to allow the XVB603 to reside in slot 1 without needing an extra system controller. The VME controller is connected via a x4 connection to the CPU root complex.

5.7.1 VMEbus Features

- x4 GEN1 PCIe Interface
- Integral FIFOs for write posting and read pre-fetching to maximize bandwidth utilization
- Programmable DMA controller with linked list support
- Complete suite of VMEbus address and transfer modes
- Master (including RMW) and Slave (including 2eSST RETRY*) transfer modes:
    - A32 / A24 / A16
    - D64 MBLT, 2eSST (Master DMA only)
    - D32 BLT (Master DMA only)
    - D32 / D16 / D8 SCT (Master DMA and Master Windows)

NOTE

PCIe transfer data sizes determine VME data size.

- Flexible register set, programmable from both the PCIe and VMEbus ports
- VMEbus system controller functionality
- Geographical addressing

TIP

The VME specification does not support power-controlled states such as S3 and S4. See Section C.4.1, "ACPI Settings" to enable/disable S3 and S4 sleep states.

5.7.2 VME Controller Registers

All the controlling registers are located in the VME Controller FPGA. The VME related registers are memory mapped. After powerup, the base address is assigned dynamically by the software.

The PCIe related registers can be found in the PCI configuration space.

5.7.3 VME Controller PCI Bus Address Space

The minimum address space that can be configured in the BIOS setup is 64 MBytes.

5.7.4 Using the VME Controller FPGA

Abaco supplies board support inclusive of a driver to operate the VME controller for Linux, VxWorks, and Windows, making operation straightforward via familiar APIs. Depending on program needs, drivers for other Operating Systems may be derivable on request.

5.7.5 VME Bridge (VME Controller) Software Guidelines

Programmers using Abaco computer Board Support Packages (BSPs) for the VME Bridge as used on the XVB603 single board computer, must be aware of requirements of the VME architecture.

The XVB603 VME Interface uses the VME Controller FPGA. This architecture interfaces the VME to the onboard SBC PCIe bus. In doing so, the user must be aware of the following guidelines as related to Software programming of the VME Interface:

Master Window Transfer Data Size: On Master data transfers, the VME data size is determined by the PCIe data access size. For example, in order to generate a 16-bit Word access on the VMEbus, the PCIe Access must be a 16-bit Word. In order to generate an 8-bit byte access on the VMEbus, the PCIe access must be an 8-bit byte.

Shared XVB603 Memory: Any XVB603 DRAM memory made available to another VME master through the VME Controller FPGA is subject to deadlock that may cause a VMEbus error unless specific precautions are taken. If onboard DRAM memory is slave to the VME, and a program on the XVB603 with slaved memory attempts to write (from the processor) to the VME through the VME Controller FPGA, then the user must first request ownership of the VME through the Device Wants Bus (DWB) Bit in the VME Controller FPGA, and be granted the VME, prior to doing writes to the VME bus.

The user may also implement other methods of gaining ownership of the VME, such as semaphores. But, regardless of the method used, when using shared memory, the user must gain exclusive VME ownership prior to generating asynchronous VME writes.

Extremely Long VME Slave Response Time: VME slave devices (or VME BERR conditions) that have a DTACK (or BERR) response time of greater than 16µ can cause Bridge Ordering rule issues with intermixed reads and writes through the VME Controller FPGA. If the SBC user wishes to do an extended number (larger than the depth of the VME Controller FPGA write post buffer) of consecutive writes from the processor to the VME through the VME Controller FPGA, and those writes can be intermixed with reads from another task, then the user must verify that all slaves within the system have DTACK response time of less than 16µ, and that the VME BERR timer of the system is set to 16µ max. Also, it is suggested that prior to doing any large VME transfer, the users should first request ownership of the VME through the DWB Bit in the VME Controller FPGA, and be granted the VME, prior to doing writes to the VME Controller FPGA.

The user may also implement other methods of gaining ownership of the VME, such as semaphores. But, regardless of the method used, when generating an extended number of consecutive processor-to-VME writes (larger than the depth of the write post buffer), the user must gain exclusive VME ownership prior to generating these asynchronous VME writes.

NOTE

Failure to implement the procedures outlined above may cause some system implementations to lockup or generate unwanted VME errors.

5.7.6 VME Non-Volatile Configuration

The XVB603 provides a non-volatile UEFI setup screen to adjust different VME setup options. These options include VME_SYSRESET Direction (drive as an output and/or receive as an input), SYSCON and SYSFAIL settings. See the UEFI VMEbus Configuration setup screen.

NOTE

The VME non-volatile configuration settings may always be altered in the BIOS; however, the board must be booted with the P6 jumper installed for the setting to be activated. Once activated (powerup complete), the jumper can be removed.

5.8 Interrupts

The interrupt routing for standard components such as COM1/2 is in compliance with standard PC/AT systems. Unused interrupts can be used for add-on cards or other board-specific PCI devices such as SATA and Ethernet.

Table 5-1 Interrupt Assignments

Hardware IRQ	IRQ Source
INTC1	
IRQ00	System Timer
IRQ01	Keyboard[a]
IRQ02	Cascade from INTC2
IRQ03	COM2[b]
IRQ04	COM1[b]
IRQ05	GPIO 0-7
IRQ06	Timers 1 and 2
IRQ07	COM3[b]
IRQ08	Real Time Clock
IRQ09	Power Management Control
IRQ10	Internal Use Only
IRQ11	PnP/PCI[b]
IRQ12	PS/2 Mouse[a]
IRQ13	Numeric Coprocessor
IRQ14	External SATA[c]
IRQ15	Onboard SATA[d]
NMI	Parity Error ECC Error System Error

[a] Emulated interrupt from USB keyboard/mouse.

[b] Interrupts are available for Plug and Play PCI devices

[c] This interrupt is available for other devices when the primary SATA is disabled in SETUP or when SATA is configured to native PCI-mode.

[d] This interrupt is available when the secondary SATA is disabled in SETUP or when SATA is configured to native PCI mode.

5.8.1 Interrupt Controller

The Mobile Intel CM238 Chipset provides an ISA compatible Programmable Interrupt Controller (PIC) that consists of two 82C59A devices with eight interrupt request lines each. The two controllers are cascaded so that fourteen external and two internal interrupt sources are available. The master interrupt controller provides IRQ [7...1]; the slave interrupt controller provides IRQ [15...8]. IRQ2 is used to cascade the two controllers, IRQ0 is used as a system timer interrupt and is tied to interval timer 1, counter 0. The remaining fourteen interrupt lines are mapped to various onboard devices. Each 82C59A provides several internal registers. The interrupts on the IRQ input lines are handled by two registers: the interrupt request register IRR and the in-service register ISR. For programming details see the 82C59A data sheet.

The XVB603 also supports the Interrupt handling of the Advanced Programmable Interrupt Controller (APIC). This handling of the APIC interrupt services must be supported by the operating system. The I/O APIC handles interrupts very differently than the 8259.

5.8.2 Advanced Programmable Interrupt Controller

The XVB603 supports APIC. This handling of the APIC interrupt services must be supported by the operating system. The I/O APIC handles interrupts differently than the standard interrupt controller. These differences are:

- Method of Interrupt Transmission: The I/O APIC transmits interrupts through processor FSB, and interrupts are handled without the need for the processor to run an interrupt acknowledge cycle.
- Interrupt Priority: The priority of interrupts in the I/O APIC is independent of the interrupt number. For example, interrupt 10 may be given a higher priority than interrupt 3.
- More Interrupts: The three I/O APICs in the XVB603 support a total of twenty-four independent interrupt sources.

5.8.3 Message Signaled Interrupts

The XVB603 supports Message Signaled Interrupts (MSI) on all its PCIe links for transporting interrupts from PCIe devices towards the CPU.

5.9 Timer (8254)

The XVB603 is equipped with an 8254-compatible timer. This timer contains three counters. Each counter output provides a key system function. Counter 0 is connected to interrupt controller input IRQ0 and provides a system timer interrupt for time-of-day, floppy disk time-out and other system timing functions. Counter 1 generates a refresh request signal and Counter 2 generates the sound for the speaker.

The following table gives an overview of the 8254 timer functions.

Table 5-2 Interval Timer Functions

Interval Timer Function	Description
Counter 0 (System Timer)	
Gate	Always on
Clock In	1.193 MHz (OSC/12)
Out	IRQ0 (INT1)
Counter 1 (Refresh Request)	
Gate	Always on
Clock In	1.193 MHz (OSC/12)
Out	Refresh Request
Counter 2 (Speaker Tone)	
Gate	Programmable via Port 0x061
Clock In	1.193 MHz (OSC/12)
Out	Speaker

The counter/timers are programmed by I/O accesses. A single control word register controls the operation of all three counters. For more information on programming and a detailed register description, see the 8254 data sheet.

5.10 Real Time Clock

The two key functions of the Real Time Clock (RTC) are:

1. Tracking time of day
2. Storing system data, even when the system is powered down

The PCH provides the RTC module that is equipped with a battery backed-up date and time keeping device. The RTC is powered from the +5V_STDBY or VBAT supply. When either of these supplies is present, the system clock is maintained. If all power is removed, the RTC is reset. Valid RAM date and time can be maintained after powering down using an external battery source.

The RTC module is comprised of a clock with 1 second resolution and 242 bytes of general-purpose CMOS RAM used by system UEFI Firmware. The three maskable interrupts' features are:

- Time of day alarm with once a second to once a month range

- Periodic rates of 122µs to 500ms
- End of update cycle notification

The lower 14 bytes on the lower RAM block has very specific functions. The first ten are for time and date information. The next four (0Ah to 0Dh) are registers, which configure and report RTC functions. In addition to providing time of day, the RTC provides a 100-year calendar with alarm features and battery backed operation. The time of day function includes fourteen control registers.

NOTE

The leap year determination for adding a 29th day to February does not take into account the end- of-the-century exceptions.

5.11 UEFI Firmware - Backup UEFI Firmware

The XVB603 provides two 16 MByte SPI flash devices for the UEFI firmware. The two devices consist of a primary and a recovery image. Integrated logic is used to switch between the primary and the recovery device.

Switching between primary and backup UEFI is controlled by jumper header P3. When there is no jumper on P3, then the primary UEFI is used. When a jumper is installed on P3, then the recovery UEFI is used. See Figure 2-1 for location of P3 header.

UEFI Firmware with Backup UEFI Firmware - Easy updating, in-system programmable Flash ROM, automatic system configuration.

- Integrated VBIOS, and Ethernet PXE OpROM
- USB mass storage support, password protection, headless support
- Remote console via serial port

5.12 BMC

A Baseboard Management Controller (BMC) is implemented on the XVB603, interfacing between the host processor and the system management network. This controller can also function as a Peripheral Management (PM) Controller. The BMC is mapped into the local CPU's I/O address space.

If the power of the XVB603 is off, the Intelligent Platform Management Interface (IPMI) controller may be supplied by the +5VSTDBY power pin.

For information about the System Management in VME systems, please refer to the VITA 38 and PICMG® 2.9 System Management Specification. More information about IPMI can be found at the Intel website below.

LINK

www.intel.com/content/www/us/en/servers/ipmi/ipmi-home.html.

5.12.1 IPMB

The Intelligent Platform Management Bus (IPMB) is an I^2C based bus that provides a standardized interconnection between different VME boards within a chassis. The standardized connection to the backplane is shown below.

Table 5-3 IPMB Backplane Pin Assignments

P1	Name	Description
B21	IPMB_SCL	Serial Clock
B22	IPMB_SDA	Serial Data
B31	+5VSTDBY	Power Supply for all IPMI-devices

5.12.2 SMBus

The SMBus is an I^2C-based bus that provides a standardized interconnection between the BMC and other I^2C devices on the chassis. The standardized connection to the backplane is shown below:

Table 5-4 SMBus Backplane Pin Assignments

P1	Name	Description
D19	SMB_SCL	Serial Clock
D21	SMB_SDA	Serial Data
D23	SMB_ALERT#	SMBus Alert signal to IPMI controller

5.13 Elapsed Time Indicator

A Dallas DS1682 Elapsed Time Indicator (ETI) logs the amount of time the XVB603 has been powered and the number of power cycles. Power up time is only recorded when the platform is fully powered and not in State S3, S4 or S5. Power cycle events are only recorded when the backplane +5V power rail transitions from on to off.

The ETI is intended only to be used by Abaco software drivers. See the relevant software manual for details. For more details on the ETI device, see www.maxim-ic.com.

5.14 Keyboard and Mouse

The communication between the PC and the keyboard and mouse is managed by a USB connection. A legacy 8042 interface is available via emulation for USB unaware OS. See Section 5.8, “Interrupts”.

5.15 SATA Interface

The XVB603 offers up to six SATA Gen1 and Gen2 channels that can transfer up to 300 MByte/s.

- SATA1 to Rear P2
- SATA2 to Rear P2
- SATA3 to Rear P0 (Optional based on P0 load)
- SATA4 to Rear P0 (Optional based on P0 load)
- SATA5 to Front Panel
- SATA6 to Optional Onboard M2 drive

The XVB603 UEFI Firmware automatically detects connected SATA Drives or flash disks and enters the corresponding drive parameters into the UEFI Firmware setup.

Using SATA and SCSI devices: The PC allows the simultaneous use of SATA and SCSI hard disks (for example: SCSI PMC). UEFI Firmware setup allows reordering drives to boot from either SCSI or SATA drives.

5.16 Gigabit Ethernet Interface

Four Ethernet interfaces are available on the XVB603 depending on the configuration. The ports are high performance 1000BASE-T (backward compatible with 10BASE-T/100BASE-TX).

Use of PCH Internal Gbit MAC, combined with I219 Jacksonville Gbit PHY, provides VPRO capability. All four ports provide IEEE-1588 capability. Each network interface is assigned a unique MAC address which resides in an Ethernet address ROM on the XVB603. All GbE interfaces are equipped with LEDs indicating Link and Activity.

- Two GbE interfaces available at the front panel
  - ETH1 Intel Springville, standard port
  - ETH2 Intel Springville, standard port.
- Two GbEs at the rear are routed to P0 (ANSI/VITA 31.1-2003 compliant)
  - ETH3 Intel Springville
  - ETH4 Intel Clarksville

Remote booting is supported on all four ports with Intel PXE Boot Firmware.

5.17 Additional Devices

5.17.1 XVB603 Field Programmable Gate Array Devices

The XVB603 has a Field Programmable Gate Array (FPGA) that controls the power sequence and reset sources. The FPGA also contains additional devices: Serial Ports, Watchdog Timer, NVRAM, Timers, GPIO and Board Configuration registers. See Section 7.1, "FPGA Control and Status Registers" for details.

- Serial Ports
- Watchdog Timer
- NVRAM
- Timers
- GPIO
- Board Configuration

See Section 7.1, “FPGA Control and Status Registers” for register details.

Serial Ports

The XVB603 serial ports are provided by the SmartFusion 2 FPGA. The XVB603's serial ports are fully compatible with the 16550D UART. Each serial interface provides a 16-Byte FIFO, offering higher performance than earlier used standard serial interfaces. The UARTs have programmable baud rate generators capable of up to 115200 baud. There are four address locations defined for serial interfaces on standard PCs. The serial interfaces are I/O mapped and can occupy four address ranges.

- COM1 and COM2 are available out the rear VME P2 connector and are included on all board options. COM1 and COM2 support both RS232 or RS422/485 (Selectable in BIOS setup) and provide the following serial port signals: (See Table 4-16 for VME P2 connector COM1 and COM2 signal locations.)

Table 5-5 Support for Serial Ports on Rear P2 Connector

RS232	RS422/485
TXD	TX-
RXD	RX-
CTS	RX+
RTS	TX+

- COM3 is an RS232 only interface located on the Front Panel. COM 3 is supported on all options. See Table 4-5 for COM3 connector signal names and pin locations.

NOTE

COM1 and COM2 ports support RS232, as well as RS422/485 (No onboard termination). Control for COM1-3 port settings is available in the UEFI setup screen Abaco -> FPGA Configuration.

Watchdog Timer

The XVB603 provides a Watchdog timer (WDT) in the onboard FPGA. This timer can be loaded with 8 different count values ranging from 2ms up to 67s. Once loaded and enabled, the WDT will count until the load value is reached, or the count is reset by accessing the WDT Keep Alive Register. If the Keep Alive Register is not accessed before the count is reached, the WDT will reset the XVB603. See Table 7-5.

NVRAM

The NVRAM is a 512 KByte Non-volatile memory residing at location 0xDC000000 memory space. 256 KBytes are reserved for BIT, and 256 KBytes are available for the user. The total 512 KByte space is addressed with eight 64 KByte memory pages. Memory page selection is controlled by the NVRAM register located at IO Space 0x68A. See Table 7-14 for additional details on NVRAM Page Registers.

Timers

The XVB603 FPGA provides two 32-bit timers with load, continuous and one-shot modes, and interrupt capability. See Table 7-15, Table 7-16, Table 7-22 and Table 7-23.

GPIO (0-7)

The GPIO is sourced from the FPGA. Eight GPIO pins are available on the VME connector P2. These pins can be used for I/O functions with output 3.3V signals as well as 3.3V and 5V tolerant inputs. Refer to Table 7-29 through Table 7-46 for more GPIO details.

Board Configuration

The XVB603 FPGA provides registers dedicated to providing information regarding the unit options for items such as Front panel presence, number and type of video displays, Ethernet ports, SATA ports, USB ports, etc.

Refer to Table 7-60 and Table 7-61 for more register descriptions that include board configuration registers.

5.17.2 Temperature Sensors

Temperature sensors are integrated in the CPU die, PCH die, and the sensor of the FPGA that displays the local onboard temperature of the XVB603 and is located beneath the CPU heat sink. The BMC or FPGA sensor provides an integrated over-temperature output that can be used to take actions such as reducing the CPU speed. The die sensors of the CPU and PCH may be programmed to take actions to protect the devices from overheating. The CPU temperature sensor has a catastrophic protection which shuts down the CPU core voltage if the die temperature reaches above 125 °C.

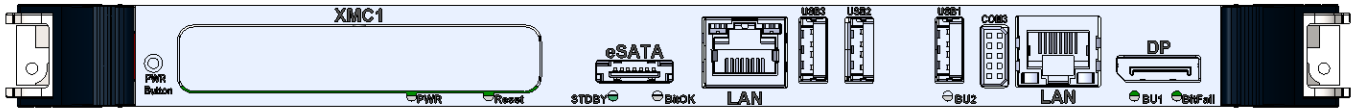
5.17.3 Geographic Addressing

If the backplane supports geographic addressing (GA), the XVB603 can detect the unique address in a VME System with the GA [5...0] pins on the VME connector P1.

5.18 LEDs

The XVB603 has a set of status LEDs for indicating power/startup and BIT status (see your Sales Representative for BIT availability). Five LEDs plus two user-programmable LEDS are available at the front panel. Two status lines for LEDs are connected to the rear. For more details on the front panel, see Section 4.1, "Front Panel Interface".

Figure 5-4 XVB603 Front Panel



5.18.1 Front I/O LEDs

Table 5-6 Front Panel LED Status Descriptions

Front Panel Marking	Related Function	LED Color	Status Description
PWR	Power Good	Green	ON – Power is good OFF – No power
Reset	Reset Status	Red	ON – Board in reset OFF – Board not in reset
STDBY	Standby Power from backplane	Green	ON – Receiving standby power (5V) from the backplane OFF – No standby power from the backplane
BitOK	BIT Pass	Green	ON – BIT Passed OFF – No BIT Pass
BU2	BIT/User Status #2	Yellow	user-programmable
BU1	BIT/User Status #1	Yellow	user-programmable
BitFail	BIT Fail	Red	ON – BIT Failed OFF – No BIT Fail

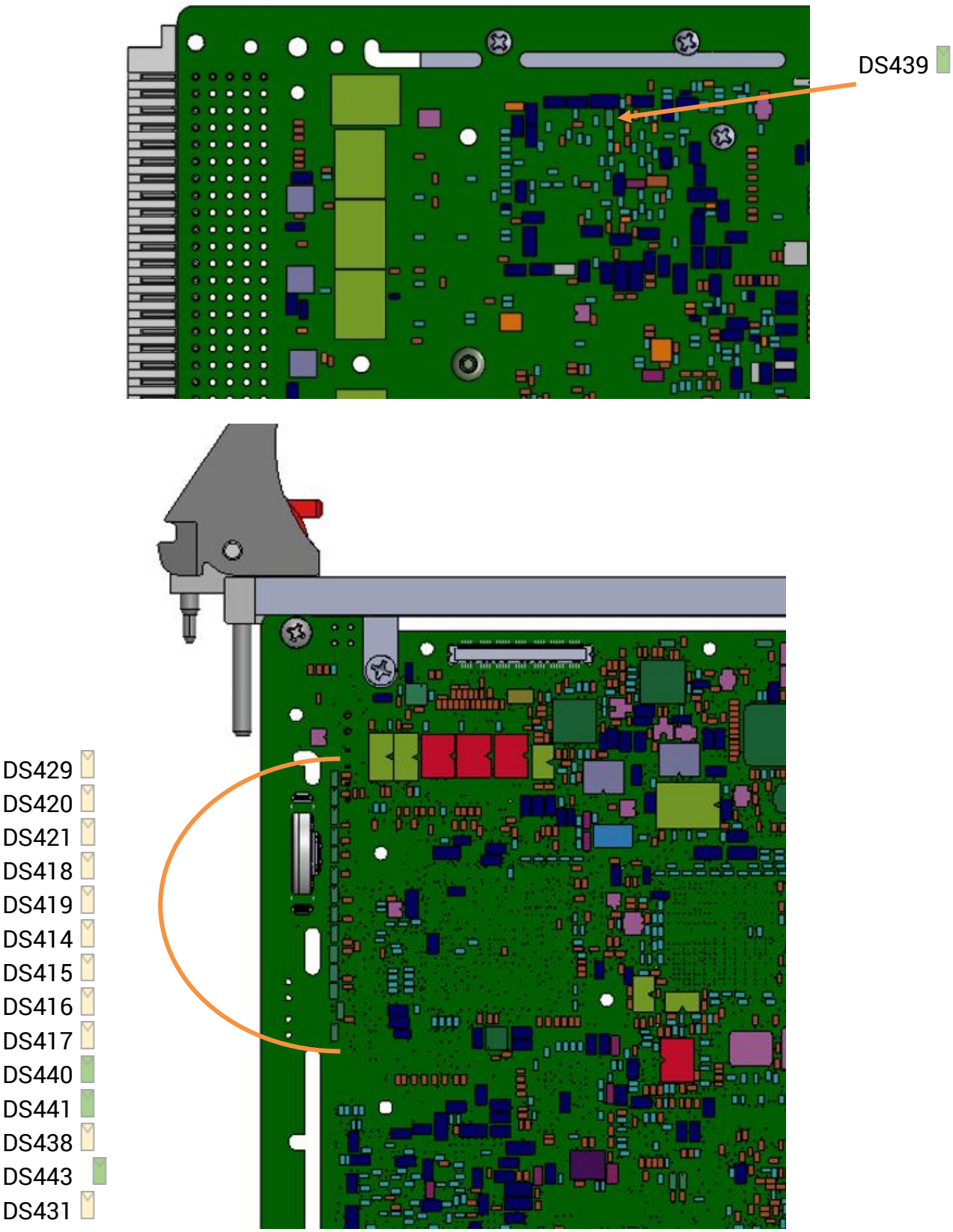
5.18.2 Rear I/O LEDs

- 1x Rear BITFail LED signal
- 1x Rear Boot Status LED signal

The rear status LED signals provide the board status for external LEDs. The signal already implements serial resistors on the XVB603.

5.18.3 Onboard LEDs – Bottom Assembly

Figure 5-5 XVB603 Bottom Assembly – LED Locations



NOTE

Bottom Assembly LEDs may not be visible on all options, or when the unit is inserted into a chassis.

Table 5-7 Onboard LEDs – Bottom Assembly

LED	Related Function	LED Color	Meaning When Lit
DS414 – DS421	POST Status	Yellow	Shows the value of the most recent PORT80 write cycle, where DS414 = bit 0 of the PORT80 register and DS421 = bit 7 of the PORT80 register
DS429	SATA Activity	Yellow	SATA device is active
DS431	Sleep Status	Yellow	The board is in sleep state S3, S4 or S5
DS438	BMM Status	Yellow	Reserved for future BMM use
DS439	VME Done	Green	For Manufacturing use only
DS440	3.3V	Green	3.3V signal present @ LED
DS441	3.3V AUX	Green	3.3V AUX signal present @ LED
DS443	5V	Green	5V signal present @ LED

6 • Memory Mapping and Registers

This chapter describes system resources, such as memory mapping and register settings.

6.1 Memory Mapping

The table below shows the memory address area used by the XVB603.

Table 6-1 Memory Mapping

Address (Hex)	Size	Used by
0 - 9_FFFF	640 KByte	System RAM
A_0000 - B_FFFF	128 KByte	Video RAM (if enabled)
C_0000 - D_FFFF	128 KByte	Used by PCI ROMs, Add-on cards
E_0000 - F_FFFF	128 KByte	UEFI Firmware
10_0000 - EFFF_FFFF	Depends on available	Extended RAM
DC00_0000 - DC00_FFFF	64 KByte	NVRAM 64 KByte Page
4000_0000 - FFBF_FFFF	Depends on available	Dynamically used by PCI devices
FF80_0000 - FFFF_FFFF	8 MByte	SPI ROM (UEFI Firmware and descriptors)

6.2 Register Settings

The following section provides an overview of the registers located in the I/O address area of the XVB603.

NOTE

The address locations of the PCI devices, such as Ethernet, are not described in the following tables. This is because the UEFI Firmware automatically configures all PCI devices.

6.2.1 Standard Register Settings

The standard register settings are equal to all standard PC/AT systems. The table below provides an overview of the address ranges occupied by these registers.

Table 6-2 Standard Register Settings

I/O Address Range (Hex)	Function
00 - 0F	DMA Controller
20 - 21	Interrupt Controller
40 - 43	Counter / Timer
60	Keyboard Controller
61	NMI Status and Control
64	Keyboard Controller
70 - 71	RTC, NMI Mask
80 - 8F	DMA Page Register
A0 - A1	Interrupt Controller
B2 - B3	Power Management
C0 - DE	DMA Controller
F0 - F1	Coprocessor
170 - 177	Secondary SATA
1F0 - 1F7	Primary SATA
2E8 - 2EF	COM port[a]
2F8 - 2FF	COM port[a]
3E8 - 3EF	COM port[a]
3F8 - 3FF	COM port[a]
600 - 6FF	XVB603 specific[b]

[a] Via setup four address ranges can be defined for the serial interfaces.

[b] Used for onboard programmable options.

7 • FPGA Registers

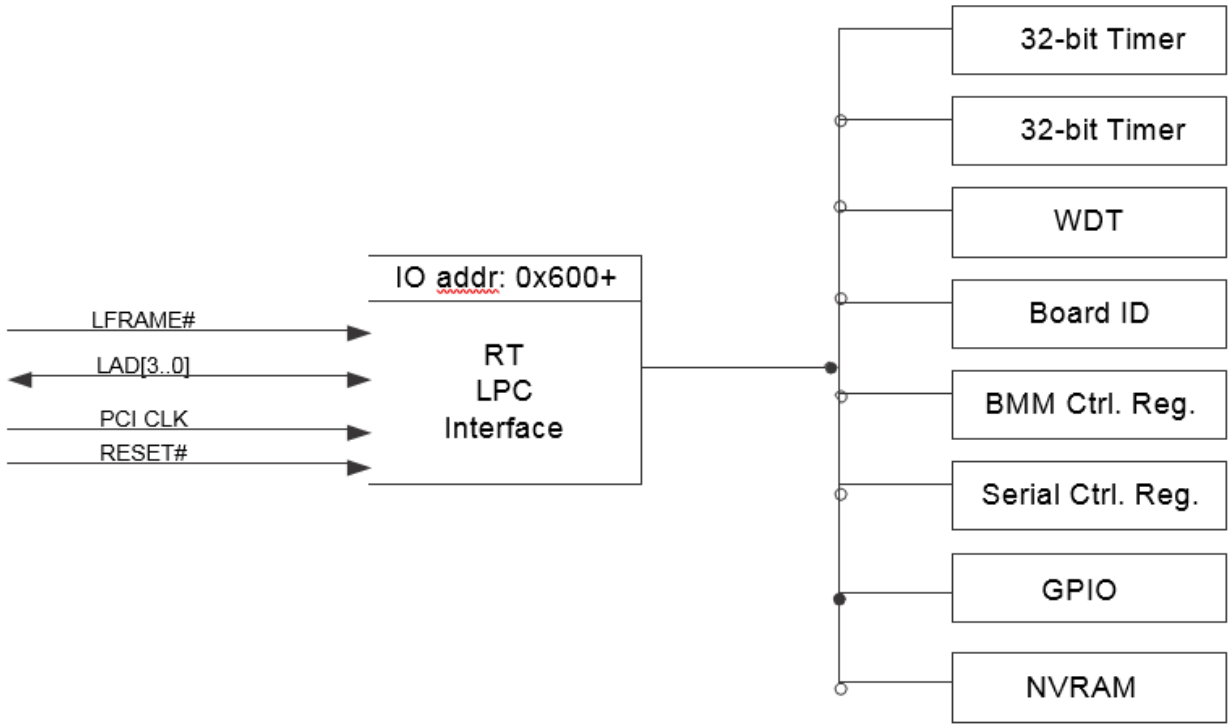
The FPGA is a device that provides the following:

- Onboard registers
- Watchdog Timer for synchronizing and controlling multiple events
- Software controlled general purpose timers
- GPIO signals sourcing
- Write protection control

The XVB603 provides bootable NAND Flash and 512 KBytes of nonvolatile random-access memory (NVRAM). 256 KBytes are reserved for BIT, and 256 KBytes are available for the user.

The block diagram for the FPGA is shown in the figure below.

Figure 7-1 Block Diagram for FPGA



7.1 FPGA Control and Status Registers

The XVB603 FPGA contains an LPC interface for access to real-time user functions such as Watchdog timer, 32-bit Timers, and GPIO. There are also control and status registers for other board functions such as BIT, Board/Front Panel Options, NVRAM Page control, and COM Port Configuration. The FPGA registers are mapped in I/O space staring at address 0x600.

See Table 7-1 for the list of XVB603 FPGA Registers.

Table 7-1 XVB603 FPGA Register Definitions

LPC I/O Port (Hex)	Description	Access
600	Board ID	Read
601	Board Revision	Read
602-60A	Reserved	N/A
60B	FPGA Revision	Read
60C	Reserved	N/A
60D	Watchdog Timers (WDT) Refresh	Read/Write
60E	WDT CSR (LSB)	Read/Write
60F	WDT CSR (MSB)	Read/Write
610-61A	Board ID String	Read
61B	Reset Cause Register 1	Read
61C	Reset Cause Register 2	Read
61D-621	Reserved	N/A
622	LED Control	Read/Write
623-624	Reserved	N/A
625	UEFI/SPI Control	Read/Write
626-628	Reserved	N/A
629	BIT Control/Status Register	Read/Write
62A-634	Reserved	N/A
635	NVRAM Memory Space Page Register	Read/write
636-64F	Reserved	N/A
650	Timer 0 CSR1	Read/Write
651	Timer 0 CSR2	Read/Write
652	Timer 0 IRQ Clear	Write to Clear
653	Reserved	N/A
654	Timer 0 Byte 0 (LSB)	Read/Write
655	Timer 0 Byte 1	Read/Write
656	Timer 0 Byte 2	Read/Write
657	Timer 0 Byte 3 (MSB)	Read/Write
658	Timer 1 CSR1	Read/Write
659	Timer 1 CSR2	Read/Write
65A	Timer 1 IRQ Clear	Write to Clear
65B	Reserved	N/A

LPC I/O Port (Hex)	Description	Access
65C	Timer 1 Byte 0 (LSB)	Read/Write
65D	Timer 1 Byte 1	Read/Write
65E	Timer 1 Byte 2	Read/Write
65F	Timer 1 Byte 3 (MSB)	Read/Write
660-66F	Reserved	N/A
670	GPIO 7-0 Out	Read/Write
671	GPIO 7-0 In	Read
672	GPIO 7-0 Direction	Read/Write
673	GPIO 7-0 Interrupt Enable	Read/Write
674	GPIO 7-0 Interrupt Level/Edge	Read/Write
675	GPIO 7-0 Interrupt Active High/Low	Read/Write
676	GPIO 7-0 Both-Edge	Read/Write
677	GPIO 7-0 Interrupt Status	Read/Write to Clear
678	GPIO 7-0 Availability	Read
679-67B	Reserved	N/A
67C	GPIO 15-8 Out	Read/Write
67D	GPIO 15-8 In	Read
67E	GPIO 15-8 Direction	Read/Write
67F	GPIO 15-8 Interrupt Enable	Read/Write
680	GPIO 15-8 Level/Edge	Read/Write
681	GPIO 15-8 Active Low/High	Read/Write
682	GPIO 15-8 Both-Edge	Read/Write
683	GPIO 15-8 Interrupt Status	Read/Write to Clear
684	GPIO 15-8 Available	Read
685-69F	Reserved	N/A
6A0	Ethernet Port Availability	Read
6A1	COM Port Availability	Read
6A2	COM Port Wire Configuration	Read
6A3	COM Port Full Modem Line Configuration	Read
6A4	SATA Port Availability	Read
6A5	USB 2.0 Port 7:0 Available	Read
6A6	USB 3.0 Port 7:0 Available	Read
6A7	USB 2.0 Port 15:8 Available	Read
6A8	USB 3.0 Port 15:8 Available	Read
6A9	Display Type Availability	Read
6AA	Display Type VGA	Read
6AB	Display Type DVI/HDMI	Read
6AC	DisplayPort Availability	Read
6AD	Ancillary/Audio Availability	Read
6AE	Front Panel Configuration	Read
6AF	PMC/XMC I/O Configuration	Read
6B0	Reserved	N/A
6B1	SSD (M.2) Availability Register	Read

LPC I/O Port (Hex)	Description	Access
6B2	SSD Hardware Secure Erase Availability (Reserved)	Read
6B3-6B7	Reserved	N/A
6B8	UART Enable	Read/Write
6B9-6BA	Reserved	N/A
6BB	COM Port Transceiver Enable	Read/Write
6BC	COM Port RS232/RS422 Selections	Read/Write
6BD	COM Port RS485 Auto Direction Control	Read/Write
6BE	COM Port Loop-back Enable	Read/Write
6BF	SSD Erase Control Register (Reserved)	Read/Write
6C0	SSD Cache Flush Control Register (Reserved)	Read/Write
6C1-6C5	Reserved	N/A
6C6	Scratch Pad Register	Read/Write
6C7	Reserved	N/A
6C8	PMC/XMC Status	Read
6C9	Reserved	N/A
6CA	VME Backplane Status	Read
6CB	Reserved	N/A
6CC	Write Protection Status	Read
6CD	Board Jumper Status	Read
6CE	Boot Location Status	Read
6CF-6F2	Reserved	N/A
6F3	CPU Daisy Chain Status/Control Register	Read/Write
6F4-6F5	Reserved	N/A
6F6	Board Power/Reset Status	Read
6F7-6FF	Reserved	N/A

Table 7-2 Board ID Register (0x600)

Bit	R/W	Description	Default
7:0	R	Returns the Value of the XVB603 board ID	0x8B

Table 7-3 Board Revision Register (0x601)

Bit	R/W	Description	Default
7:4 0x0=Rev 1 0x2=Rev 2	R	Major assembly revision (artwork)	N/A
3:0 0x0=Rev A, 0x1=Rev B	R	Minor revision (Hardware build state revision	N/A

Table 7-4 FPGA Revision Register (0x60B)

Bit	R/W	Description	Default
7:0	R	Revision of FPGA code	N/A

Table 7-5 Watchdog Timer (WDT) Refresh (0x60D)

Bit	R/W	Description	Default
7:0	R/W	Any Write access to this register will re-load the Watchdog Timer.	0x00

Table 7-6 WDT Control/Status Register (CSR) LSB (0x60E)

Bit	R/W	Description	Default
7:1	R	Reserved	N/A
0	R/W	Watchdog Timer Count Enable 1 = WDT enabled 0 = WDT disabled)	0

Table 7-7 WDT Control/Status Register (CSR) MSB (0x60F)

Bit	R/W	Description	Default
7:3	R	Reserved	N/A
2:0	R/W	Watchdog Timer Timeout Selection 111= WDT Timeout = 2mS 110= WDT Timeout = 32mS 101= WDT Timeout = 131mS 100= WDT Timeout = 262mS 011= WDT Timeout = 524mS 010= WDT Timeout = 2.1S 001= WDT Timeout = 33S 000= WDT Timeout = 66S	111

Table 7-8 Board ID String Registers (0x610 - 0x61A)

Bit	R/W	Description	Default
7:0	R	These bytes read back ASCII values for "XVB603" 0x610=0x58 ("X") 0x611=0x56 ("V") 0x612=0x42 ("B") 0x613=0x36 ("6") 0x614=0x30 ("0") 0x615=0x33 ("3")	 0X58 0x56 0x42 0x36 0x30 0x33

Table 7-9 Reset Cause Register 1 (0x61B)

Bit	R/W	Description	Default
7-3	R	Reserved	N/A
2	R	Reserved for Front Panel Reset	N/A
1	R	Reserved	N/A
0	R	VME Reset	0

Table 7-10 Reset Cause Register 2 (0x61C)

Bit	R/W	Description	Default
7	R	BMM Reset	0
6	R	Reserved	N/A
5	R	PLT Reset	0
4	R	XMC Reset	0
3	R	XDP Reset	0
2	R	Watchdog Reset	0
1	R	TAC Reset	0
0	R	Reserved	N/A

Table 7-11 LED Control Register (0x622)

Bit	R/W	Description	Default
7	R/W	BIT PASS LED 1 = LED ON 0 = LED OFF	0 (sticky on BIT reset)
6	R/W	BIT Fail LED 1 = LED ON 0 = LED OFF **See Note and Caution below**.	0 (sticky on BIT reset)
5	R/W	BIT/User Status 1 LED 1 = LED ON 0 = LED OFF	0
4	R/W	BIT/User Status 2 LED 1 = LED ON 0 = LED OFF	0
3:0	R	Reserved	N/A

NOTE

This output is OR'ed with the BMC BIT FAIL output before driving the LED and the BIT_FAIL pin on the backplane.

CAUTION

Writing to bit 6 of the LED Control register is not recommended. Writes to this bit may contradict BIOS and/or power-on BIT status.

Table 7-12 UEFI/SPI Control Register (0x625)

Bit	R/W	Description	Default
7	R/W	Select Other boot device 1 = Opposite boot device from which the board was booted is selected (i.e., if booted from recovery, main device is selected) 0 = Boot device from which the board was booted is selected	0
6	R	Reserved	N/A
5	R	FSP Selected Status 1 = FSP selected 0 = FSP not selected	0
4	R	Powerup DIPSW Default Boot 1 = FSP selected to boot at powerup 0 = BIOS selected to boot at powerup	0
3	R/W	Boot FSP on Reset 1 = FSP selected to boot at powerup 0 = BIOS selected to boot at powerup	0
2	R/W	SPI CSn MUX Override 1 = Override SPI Flash CSn operation 0 = Normal SPI Flash operation	0
1-0	R/W	SPI CSn MUX Override Select 00 = Main Boot Flash 01 = Recovery Boot Flash 10 = FSP/BIT Boot Flash 11 = Main Boot Flash	00

Table 7-13 BIT Control/Status Register (0x629)

Bit	R/W	Description	Default
7	R/W	HRESET 1 = Board reset requested 0 = Board reset not requested	0
6-5	R/W	Bit Run Status 00 = BIT not previously run 01 = Fast BIT performed 10 = Full BIT performed 11 = Fast Start Performed	0 (sticky when reset using HRESET req)
4	R/W	Pass/Fail 1 = Failed 0 = Passed	1 (sticky when reset using HRESET req)
3	R/W	FAST BIT enable 1 = Fast BIT enabled (via UEFI setting) 0 = Fast BIT disabled	0
2	R/W	FAST Start enable 1 = Fast Start enabled (Via UEFI setting) 0 = Fast Start Disabled	0
1	R	Reserved	N/A
0	R/W	BIT Run 1 = BIT has been run 0 = BIT not been run	0 (sticky when reset using HRESET req)

Table 7-14 NVRAM Memory Space Page Register (0x635)

Bit	R/W	Description	Default
7-3	R	Reserved	N/A
2	R/W	BIT/User NVRAM access Controls NVRAM address 18 Driven onto NVRAM bus when NVRAM is accessed 1 = 256 KByte BIT NVRAM Access 0 = 256 KByte User NVRAM Access	0
1:0	R/W	64 KByte page select NVRAM address 17:16 Driven onto NVRAM bus when NVRAM is accessed	0

Table 7-15 Timer 0 Control and Status Register 1 (CSR1) (0x650)

Bit	R/W	Description	Default
7	R	Timer IRQ status 1 = Pending 0 = No Interrupt	N/A
6	R	Reserved	N/A
5:4	R/W	Clock Source Select: 00 = Use 2 MHz FPGA Clock (default) 01 = Reserved 10 = Reserved 11 = Reserved	0

Bit	R/W	Description	Default
3	R/W	Timer Read Selection 1 = Read Timer Load Value 0 = Read Current Time Value	0
2:1	R/W	Clock Divider (Value when 2 MHz Clock used) 00 = 1:1 (2 MHz) 01 = 1:2 (1 MHz) 10 = 1:4 (500 KHz) 11 = 1:8 (250 KHz)	0
0	R/W	Enable Timer IRQ 1 = IRQ Enabled 0= IRQ Masked	0

Table 7-16 Timer 0 Control and Status Register 2 (CSR2) (0x651)

Bit	R/W	Description	Default
7:2	R	Reserved	N/A
1	R/W	Timer One-Shot Enable 1 = Timer will count down once and stop 0 = Timer will count down and reload at terminal count	0
0	R/W	1 = Timer Enabled 0 = Timer Disabled	0

Table 7-17 Timer 0 IRQ Clear Register (0x652)

Bit	R/W	Description	Default
7:0	W	Any Write to this register will clear the Timer IRQ	N/A

Table 7-18 Timer 0 Data Byte 0 (LSB) (0x654)

Bit	R/W	Description	Default
7:0	R/W	Read value depends on value of CSR1(3). If '0' - Contains Bits 7-0 of the Timer current counter value If '1' - Contains Bits 7-0 of the Timer load value Reading this register latches the upper bits of the count value to prevent rollover. Write always updates Timer load value.	0x00

Table 7-19 Timer 0 Data Byte 1 (0x655)

Bit	R/W	Description	Default
7:0	R/W	Read value depends on value of CSR1(3). If '0' - Contains Bits 15-8 of the Timer current counter value If '1' - Contains Bits 15-8 of the Timer load value Reading this register latches the upper bits of the count value to prevent rollover. Write always updates Timer load value.	0x00

Table 7-20 Timer 0 Data Byte 2 (0x656)

Bit	R/W	Description	Default
7:0	R/W	Read value depends on value of CSR1(3). If '0' - Contains Bits 23-16 of the Timer current counter value If '1' - Contains Bits 23-16 of the Timer load value Reading this register latches the upper bits of the count value to prevent rollover. Write always updates Timer load value.	0x00

Table 7-21 Timer 0 Data Byte 3 (MSB) (0x657)

Bit	R/W	Description	Default
7:0	R/W	Read value depends on value of CSR1(3). If '0' - Contains Bits 31-24 of the Timer current counter value If '1' - Contains Bits 31-24 of the Timer load value Reading this register latches the upper bits of the count value to prevent rollover. Write always updates Timer load value.	0x00

Table 7-22 Timer 1 Control and Status Register 1 (CSR1) (0x658)

Bit	R/W	Description	Default
7	R	Timer IRQ status 1 = Pending 0 = No Interrupt	N/A
6	R	Reserved	N/A
5:4	R/W	Clock source select: 00 = Use 2 MHz FPGA Clock (default) 01 = Reserved 10 = Reserved 11 = Reserved	0
3	R/W	Timer Read selection 1 = Read Timer Load value 0 = Read Current Time value	0
2:1	R/W	Clock divider (Value when 2 MHz Clock Used) 00 = 1:1 (2 MHz) 01 = 1:2 (1 MHz) 10 = 1:4 (500 KHz) 11 = 1:8 (250 KHz)	0
0	R/W	Enable Timer IRQ 1 = IRQ Enabled 0= IRQ Masked	0

Table 7-23 Timer 1 Control and Status Register 2 (CSR2) (0x659)

Bit	R/W	Description	Default
7:2	R	Reserved	N/A
1	R/W	Timer On-Shot Enable 1 = Timer will count down once and stop 0 = Timer will count down and reload at terminal count	0

Bit	R/W	Description	Default
0	R/W	Timer Enable 1 = Timer enabled 0 = Timer disabled	0

Table 7-24 Timer 1 IRQ Clear Register (0x65A)

Bit	R/W	Description	Default
7:0	W	Any write to this register will clear the Timer IRQ	N/A

Table 7-25 Timer 1 Data Byte 0 (LSB) (0x65C)

Bit	R/W	Description	Default
7:0	R/W	Read value depends on CSR1(3) If '0' - Contains Bits 7-0 of the Timer current counter value If '1' - Contains Bits 7-0 of the Timer load value Reading this register latches the upper bits of the count value to prevent rollover. Write always updates Timer load value.	0x00

Table 7-26 Timer 1 Data Byte 1 (0x65D)

Bit	R/W	Description	Default
7:0	R/W	Read value depends on CSR1(3) If '0' - Contains Bits 15-8 of the Timer current counter value If '1' - Contains Bits 15-8 of the Timer load value Reading this register latches the upper bits of the count value to prevent rollover. Write always updates Timer load value.	0x00

Table 7-27 Timer 1 Data Byte 2 (0x65E)

Bit	R/W	Description	Default
7:0	R/W	Read value depends on CSR1(3) If '0' - Contains Bits 23-16 of the Timer current counter value If '1' - Contains Bits 23-16 of the Timer load value Reading this register latches the upper bits of the count value to prevent rollover. Write always updates Timer load value.	0x00

Table 7-28 Timer 1 Data Byte 3 (MSB) (0x65F)

Bit	R/W	Description	Default
7:0	R/W	Read value depends on CSR1(3). If '0' - Contains Bits 31-24 of the Timer current counter value If '1' - Contains Bits 31-24 of the Timer load value Reading this register latches the upper bits of the count value to prevent rollover. Write always updates Timer load value.	0x00

Table 7-29 GPIO 7-0 OUT Register (0x670)

Bit	R/W	Description	Default
7:0	R/W	GPIO7:GPIO0	0x00

The value of this register is driven onto the GPIO pins when the direction mode is set to output.

Table 7-30 GPIO 7-0 IN Register (0x671)

Bit	R/W	Description	Default
7:0	R	GPIO7:GPIO0	0x00

This register returns the status of the GPIO pins, regardless of the direction mode.

Table 7-31 GPIO 7-0 Direction Register (0x672)

Bit	R/W	Description	Default
7:0	R/W	GPIO7:GPIO0 1 = Output 0 = Input	0x00

Table 7-32 GPIO 7-0 Interrupt Enable Register (0x673)

Bit	R/W	Description	Default
7:0	R/W	GPIO7:GPIO0 1 = Interrupt enabled 0 = Interrupt masked	0x00

Table 7-33 GPIO 7-0 Interrupt Level/Edge Register (0x674)

Bit	R/W	Description	Default
7:0	R/W	GPIO7:GPIO0 1 = Edge 0 = Level	0x00

This interrupt sets the interrupt detection sensitivity of each interrupt pin (level or edge mode).

Table 7-34 GPIO 7-0 Interrupt Active High/Low Register (0x675)

Bit	R/W	Description	Default
7:0	R/W	GPIO7:GPIO0 1 = Active high / rising edge 0 = Active low / falling edge Note: Function depends on whether the bit is in level or edge mode.	0x00

This interrupt sets the interrupt detection sensitivity of each interrupt pin (active high/low or rising/falling edge depending on sensitivity mode).

Table 7-35 GPIO 7-0 Both-Edge Register (0x676)

Bit	R/W	Description	Default
7:0	R/W	GPIO7:GPIO0 1 = Both-edge mode enabled 0 = Both-edge mode disabled Note: The GPIO bit must be in edge mode for both-edge mode to work.	0x00

When enabled, both-edge mode causes interrupts to be generated on both rising and falling edges

Table 7-36 GPIO 7-0 Interrupt Status Register (0x677)

Bit	R/W	Description	Default
7:0	R/W	GPIO7:GPIO0 (Write 1 to Clear) 1 = Interrupt pending 0 = No interrupt	0x00

Table 7-37 GPIO 7-0 Availability Register (0x678)

Bit	R/W	Description	Default
7	R	GPIO7 Availability 1 = GPIO7 Available 0 = GPIO7 Not Available	N/A
6	R	GPIO6 Availability 1 = GPIO6 Available 0 = GPIO6 Not Available	N/A
5	R	GPIO5 Availability 1 = GPIO5 Available 0 = GPIO5 Not Available	N/A
4	R	GPIO4 Availability 1 = GPIO4 Available 0 = GPIO4 Not Available	N/A
3	R	GPIO3 Availability 1 = GPIO3 Available 0 = GPIO3 Not Available	N/A
2	R	GPIO2 Availability 1 = GPIO2 Available 0 = GPIO2 Not Available	N/A
1	R	GPIO1 Availability 1 = GPIO1 Available 0 = GPIO1 Not Available	N/A
0	R	GPIO0 Availability 1 = GPIO0 Available 0 = GPIO0 Not Available	N/A

This register allows software to easily determine which GPIO 7-0 signals are available on the board. All GPIO signals use shared backplane pins and are only available when the board is configured with the appropriate build option.

Table 7-38 GPIO 15-8 OUT Register (0x67C)

Bit	R/W	Description	Default
7:0	R/W	GPIO15:GPIO8	0x00

The value of this register is driven onto the GPIO pins when the direction mode is set to output.

Table 7-39 GPIO 15-8 IN Register (0x67D)

Bit	R/W	Description	Default
7:0	R	GPIO15:GPIO8	0x00

This register returns the status of the GPIO pins, regardless of the direction mode.

Table 7-40 GPIO 15-8 Direction Register (0x67E)

Bit	R/W	Description	Default
7:0	R/W	GPIO15:GPIO8 1 = Output 0 = Input	0x00

Table 7-41 GPIO 15-8 Interrupt Enable Register (0x67F)

Bit	R/W	Description	Default
7:0	R/W	GPIO15:GPIO8 1 = Interrupt enabled 0 = Interrupt masked	0x00

Table 7-42 GPIO 15-8 Interrupt Level/Edge Register (0x680)

Bit	R/W	Description	Default
7:0	R/W	GPIO15:GPIO8 1 = Edge 0 = Level	0x00

This interrupt sets the interrupt detection sensitivity of each interrupt pin (level or edge mode).

Table 7-43 GPIO 15-8 Interrupt Active High/Low Register (0x681)

Bit	R/W	Description	Default
7:0	R/W	GPIO15:GPIO8 1 = Active high / rising edge 0 = Active low / falling edge Note: Function depends on whether the bit is in level or edge mode.	0x00

This interrupt sets the interrupt detection sensitivity of each interrupt pin (active high/low or rising/falling edge depending on sensitivity mode).

Table 7-44 GPIO 15-8 Both-Edge Register (0x682)

Bit	R/W	Description	Default
7:0	R/W	GPIO15:GPIO8 1 = Both-edge mode enabled 0 = Both-edge mode disabled Note: The GPIO bit must be in edge mode for both-edge mode to work.	0x00

When enabled, both-edge mode causes interrupts to be generated on both rising and falling edges.

Table 7-45 GPIO 15-8 Interrupt Status Register (0x683)

Bit	R/W	Description	Default
7:0	R/W	GPIO15:GPIO8 (Write 1 to Clear) 1 = Interrupt pending 0 = No interrupt	0x00

Table 7-46 GPIO 15-8 Availability Register (0x684)

Bit	R/W	Description	Default
7	R	GPIO15 Availability 1 = GPIO15 Available 0 = GPIO15 Not Available	N/A
6	R	GPIO14 Availability 1 = GPIO14 Available 0 = GPIO14 Not Available	N/A
5	R	GPIO13 Availability 1 = GPIO13 Available 0 = GPIO13 Not Available	N/A
4	R	GPIO12 Availability 1 = GPIO12 Available 0 = GPIO12 Not Available	N/A
3	R	GPIO11 Availability 1 = GPIO11 Available 0 = GPIO11 Not Available	N/A
2	R	GPIO10 Availability 1 = GPIO10 Available 0 = GPIO10 Not Available	N/A
1	R	GPIO9 Availability 1 = GPIO9 Available 0 = GPIO9 Not Available	N/A
0	R	GPIO8 Availability 1 = GPIO8 Available 0 = GPIO8 Not Available	N/A

This register allows software to easily determine which GPIO 7-0 signals are available on the board. All GPIO signals use shared backplane pins and are only available when the board is configured with the appropriate build option.

Table 7-47 Ethernet Port Availability Register (0x6A0)

Bit	R/W	Description	Default
7:0	R	Ethernet ports 7:0 availability 0 = Ethernet 3.82"t port is not available 1 = Ethernet port is available	N/A

NOTE

Even when a port is not available due to a build option, the port may still be visible to software. Availability of these ports is build option-dependent.

Table 7-48 COM Port Availability Register (0x6A1)

Bit	R/W	Description	Default
7:0	R	COM 8:1 Availability 0 = COM8:1 is not available 1 = COM8:1 port is available	N/A

Table 7-49 COM Port Wire Configuration Register (0x6A2)

Bit	R/W	Description	Default
7:0	R	COM Port 8:1 4 Wire Configuration 0 = COM Port is available in 2-wire (TX/RX) mode only 1 = COM Port is available in 4-wire (RS232 or RS422) mode	N/A

Table 7-50 COM Port Full Modem Line Configuration Register (0x6A3)

Bit	R/W	Description	Default
7:0	R	COM Port 8:1 Modem Configuration 1 = Full modem line support is available 0 = Full modem line support is not available	N/A

Table 7-51 SATA Port Availability Register (0x6A4)

Bit	R/W	Description	Default
7:0	R	SATA Ports 7:0 availability 1 = SATA ports are available 0 = SATA ports are not available	N/A

Table 7-52 USB 2.0 Port 7:0 Availability Register (0x6A5)

Bit	R/W	Description	Default
7:0	R	USB 2.0 ports 7:0 availability 1 = USB 2.0 ports are available 0 = USB 2.0 ports are not available	N/A

Table 7-53 USB 3.0 Port 7:0 Availability Register (0x6A6)

Bit	R/W	Description	Default
7:0	R	USB 3.0 ports 7:0 availability 1 = USB 3.0 ports are available 0 = USB 3.0 ports are not available	N/A

Table 7-54 USB 2.0 Port 15:8 Availability Register (0x6A7)

Bit	R/W	Description	Default
7:0	R	USB 2.0 ports 15:8 availability 1 = USB 2.0 ports are available 0 = USB 2.0 ports are not available	N/A

Table 7-55 USB 3.0 Port 15:8 Availability Register (0x6A8)

Bit	R/W	Description	Default
7:0	R	USB 3.0 ports 15:8 availability 1 = USB 3.0 ports are available 0 = USB 3.0 ports are not available	N/A

Table 7-56 Display Type Availability Register (0x6A9)

Bit	R/W	Description	Default
7:4	R	Reserved	N/A
3:0	R	Display availability Bit 3 = DisplayPort Bit 2 = DVI1 Bit 1 = DVI0 Bit 0* = Embedded DisplayPort	

Table 7-57 VGA Display Availability Register (0x6AA)

Bit	R/W	Description	Default
7:0	R	Display 7:0 VGA availability 1 = Display is VGA type 0 = Display is not VGA type	N/A

Table 7-58 DVI/HDMI Availability Register (0x6AB)

Bit	R/W	Description	Default
7:3	R	Reserved	N/A
2	R	DVI1 Availability 1 = DVI1 available 0 = DVI1 not available	N/A
1	R	DVI0 Availability 1 = DVI0 available 0 = DVI0 not available	N/A
0	R	Reserved	N/A

Table 7-59 DisplayPort Availability Register (0x6AC)

Bit	R/W	Description	Default
7:4	R	Reserved	N/A
3	R	DisplayPort Availability 1 = DP available 0 = DP not available	N/A
2:0	R	Reserved	N/A

Table 7-60 Ancillary/Audio Availability Register (0x6AD)

Bit	R/W	Description	Default
7	R	Front Panel I/O available 1 = Front Panel I/O 0 = No Front Panel I/O	N/A

Bit	R/W	Description	Default
6-5	R	Reserved	N/A
4	R	COM Port 4 present on front panel 1 = COM Port 4 present 0 = COM Port 4 not present	N/A
3	R	COM Port 3 present on front panel 1 = COM Port 3 present 0 = COM Port 3 not present	N/A
2	R	COM Port 2 present on front panel 1 = COM Port 2 present 0 = COM Port 2 not present	N/A
1	R	COM Port 1 present on front panel 1 = COM Port 1 present 0 = COM Port 1 not present	N/A
30	R	Audio available 1 = Audio is available 0 = Audio is not available	N/A

Table 7-61 Front Panel Configuration Register (0x6AE)

Bit	R/W	Description	Default
7	R	eSATA present on front panel 1 = SATA present 0 = SATA not present	N/A
6	R	Ethernet Port 3 present on front panel 1 = Ethernet Port 3 present 0 = Ethernet Port 3 not present	N/A
5	R	USB 3.0 Port 1 present on front panel 1 = USB 3.0 Ports 1 & 2 present 0 = USB 3.0 Ports 1 & 2 not present	N/A
4	R	Reserved	N/A
3	R	USB 3.0 port 0 present on front panel 1 = USB 3.0 Port 0 present 0 = USB 3.0 Port 0 not present	N/A
2	R	COM3 present on front panel 1 = COM3 present 0 = COM3 not present	N/A
1	R	Ethernet port 0 present on front panel 1 = Ethernet Port 0 present 0 = Ethernet Port 0 not present	N/A
0	R	DisplayPort Video present on front panel 1 = DP video present 0 = DP video not present	N/A

Table 7-62 XMC/PMC I/O Configuration Register (0x6AF)

Bit	R/W	Description	Default
7	R	P64s compliant configuration 1 = I/O is P64 compliant 0 = I/O is not P64 compliant	N/A
6	R	Reduced P64s configuration 1 = I/O is a subset of P64 0 = I/O is not a subset of P64	N/A
5:4	R	Reserved	N/A
3	R	XMC X12d configuration 1 = I/O is X12d compliant 0 = I/O is not X12d compliant	N/A
2	R	XMC X8d configuration 1 = I/O is X8d compliant 0 = I/O is not X8d compliant	N/A
1	R	XMC X24s configuration 1 = I/O is X24s compliant 0 = I/O is not X24s compliant	N/A
0	R	XMC X38s configuration 1 = I/O is X38s compliant 0 = I/O is not X38s compliant	N/A

Table 7-63 SSD (M.2) Availability Register (0x6B1)

Bit	R/W	Description	Default
7:0	R	SSD7:SSD0 (M.2) availability 1 = SSD (M.2) available 0 = SSD (M.2) not available	N/A

Table 7-64 SSD Hardware Secure Erase Availability (Reserved) (0X6B2)

Bit	RW	Description	Default
7:0	R	SSD7:0 Secure Erase capability (Not available on the XVB603) 0 = Hardware Secure Erase (Not available on the XVB603)	0x00

Table 7-65 UART Enable Register (0x6B8)

Bit	R/W	Description	Default
7:0	R/W	COM8:1 UART Enable 1 = UART is enabled 0 = UART is disabled and will not respond to reads or writes.	N/A

Table 7-66 COM Port Transceiver Enable Register (0x6BB)

Bit	R/W	Description	Default
7:0	R/W	COM8:1 Enable 1 = COM Port transceivers enabled 0 = COM Port transceivers disabled Software should set this bit to a '1' after the desired COM port mode (i.e. RS232/RS422) is set.	N/A

Table 7-67 COM Port Mode Register (0x6BC)

Bit	R/W	Description	Default
7-4	R/W	COM8:1 mode 1 = COM Port transceiver in RS422 mode 0 = COM Port transceiver in RS232 mode	N/A

Table 7-68 COM Port RS485 Auto Direction Control Enable Register (0x6BD)

Bit	R/W	Description	Default
7:0	R/W	COM8:1 RS485 Auto Direction Control mode 1 = COM Port RS485 Auto Direction Control enabled. When enabled, this mode causes the RTS signal to assert and enable the transceiver whenever there is data ready to be transmitted on the port. Otherwise, the transceiver is tri-stated. 0 = COM Port RS485 Auto Direction Control disabled. Note: This bit can only be set to a '1' when the corresponding bit in the COM port Mode register (0x6BC) is set to "RS422 mode".	0x00

Table 7-69 COM Port Loopback Enable Register (0x6BE)

Bit	R/W	Description	Default
7:0	R/W	COM8:1 Loopback Enable 1 = COM Port transceiver loopback mode enabled 0 = COM Port transceiver loopback mode disabled (normal operation) Loopback mode can be used by test software to test the basic functionality of the transceiver.	0x00

Table 7-70 SSD Erase Control Register (Reserved) (0x6BF)

Bit	R/W	Description	Default
7:0	R/W	SSD7:0 Hardware erase (Not available on the XVB603) 0 = Hardware Erase pin negated	0x00

NOTE

To trigger a fast erase, enable bit must be written with a '1','0','1' pattern on consecutive write cycles to this register. This is to protect against "accidental" erase functions. The value read from this register represents the state of the output and not the last value written.

Table 7-71 SSD Cache Flush Control Register (Reserved) (0x6C0)

Bit	R/W	Description	Default
7:0	R/W	SSD7:0 Cache Flush (Not available on the XVB603) 0 = Cache Flush pin negated This bit directly controls the cache flush pin of the SSD device.	0x00

Table 7-72 Scratch Pad Register (0x6C6)

Bit	R/W	Description	Default
7:0	R/W	SCRATCH_PAD7:SCRATCH_PAD0	0x00

Table 7-73 PMC/XMC Status Register (0x6C8)

Bit	R/W	Description	Default
7	R	XMC Presence 1 = XMC is installed 0 = XMC is not installed	N/A
6	R	XMC VPWR voltage 0 = XMC VPWR rail is 5V 1 = XMC VPWR rail is 12V	N/A
5	R	XMC BIST status 1 = XMC BIST is active 0 = XMC BIST is not active	N/A
4:3	R	Reserved	N/A
2	R	PMC enumeration-ready status 1 = PMC ERDY pin is active (OK to enumerate) 0 = PMC ERDY pin is not active	N/A
1	R	PMC VIO voltage 1 = PMC VIO voltage = 5V 0 = PMC VIO voltage = 3.3V	N/A
0	R	PMC Presence 1 = PMC is installed 0 = PMC is not installed	N/A

Table 7-74 VME Backplane Status Register (0x6CA)

Bit	R/W	Description	Default
7	R	VME System Controller Status 1 = Is System Controller 0 = Is Not System Controller	N/A
6	R	VME NVMRO Status 0 = Write Protected 1 = Write Enabled	N/A
5	R	VME Geographical Address Parity	N/A
4:0	R	VME Geographical Address	N/A

Table 7-75 Write Protection Status Register (0x6CC)

Bit	R/W	Description	Default
7	R	PCIe to PCI-X Bridge EEPROM status 1 = Write protected 0 = Not Write protected	0
6	R	Ethernet SPI status 1 = Write protected 0 = Not Write protected	0
5	R	SPD EEPROM status 1 = Write protected 0 = Not Write protected	0
4	R	Reserved	N/A
3	R	Boot SPI status 1 = Write protected 0 = Not Write protected	0
2	R	Recover Boot SPI status 1 = Write protected 0 = Not Write protected	0
1	R	NVRAM status 1 = Write protected 0 = Not Write protected	0
0	R	Reserved	N/A

Table 7-76 Board Jumper Status Register (0x6CD)

Bit	R/W	Description	Default
7	R	Reserved	N/A
6	R	Backup UEFI jumper status 1 = Jumper is installed 0 = Jumper is not installed	0
5	R	Write protect jumper status 1 = Jumper is installed 0 = Jumper is not installed	0
4:0	R	Reserved	N/A

Table 7-77 Board Location Status Register (0x6CE)

Bit	R/W	Description	Default
7	R	Reserved for Auto swap fail over	0
6:5	R	Active Boot ROM location 1x = Active boot ROM is located on the test card (FACTORY ONLY) 00 = Active boot ROM is the Main onboard ROM 01 = Active boot ROM is the Recovery onboard ROM	0
4	R	SPD Location 1 = Board booted using SPD EEPROMs located on test card 0 = Board booted using SPD EEPROMs located onboard Determined by the state of the TAC SPD jumper on the test card	0
3	R	Ethernet configuration ROM location 1 = Board booted using ethernet configuration ROM on test card	0

Bit	R/W	Description	Default
		0 = Board booted using ethernet configuration ROM onboard.	
2:0	R	Reserved	N/A

Table 7-78 CPU Daisy Chain Status/Control Register (0x6F3)

Bit	R/W	Description	Default
7:5	R	Reserved for future use.	N/A
4	R	Daisy Chain Receive Status when bit 0 of this register set Low: 1 = Daisy chain has failed (open circuit or short to VCC) 0 = Daisy chain status OK when bit 0 of this register set High: 1 = Daisy chain status OK 0 = Daisy chain has failed (short circuit to GND)	N/A
3:1	R	Reserved for future use	N/A
0	RW	Daisy chain drive 1 = Drive daisy chain track High 0 = Drive daisy chain track Low	0

Table 7-79 Board Power/Reset Status Register (0x6F6)

Bit	R/W	Description	Default
7	R	Power/reset status register valid 0 = Register not supported. All other bits are invalid. 1 = Register supported. Bits 6:0 return valid data.	1
6:4	R	Reserved for future use	N/A
3	R	Board Reset status. 0 = Board Reset signal not asserted 1 = Board Reset signal asserted	N/A
2:1	R	Reserved for board-specific use	N/A
0	R	Board PWROK signal status 0 = Board PWROK signal not asserted 1 = Board PWROK signal asserted Board PWROK is asserted to indicate that all required onboard and backplane supplies are within specification. The PWRGOOD LED is driven from this signal.	N/A

A • Specifications

A.1 Mechanical

Table A-1 Mechanical Construction

Aspect	Details
Form Factor	6U, single slot, 4HP
PCB	FR4 Multilayer
Dimensions*	233.35 mm x 178 mm x 20 mm
Weight	1.38 lb

* Measured from the backplane connector mounting plane to the front panel face.

A.2 RoHS Compliance

XVB603 is RoHS compliant.

A.3 Reliability (MTBF)

The following table shows the predicted values for reliability as Mean Time Between Failures (MTBF) and failures per million hours (fpmh) for the XVB603-24210010 (contact the Abaco Sales Team for variant details) as 16 February 2017. Abaco employs the base equations, with default values in MIL-HDBK-217F(N2) Appendix A, but where the component's BOM description offers specific information (e.g. wattage, capacitance, dielectric, frequency etc.) this is used in the base equations instead of the defaults. Every effort is made to seek manufacturer's reliability data for microcircuits and where available, microcircuit manufacturer's data is used instead of MIL-HDBK-217(N2) data according to the guidance in Appendix H of VITA 51.1-2008 (2013).

Table A-2 XVB603 Reliability (MTBF)

Environment	Temp	T_J	Failure Rate (fpmh)	MTBF (hours)
Ground Benign	30°C	50°C	2.435687	410,562
Ground Fixed	40°C	60°C	12.824123	77,978
Ground Mobile	45°C	65°C	30.687098	32,587
Naval Sheltered	40°C	60°C	15.289486	65,404
Naval Unsheltered	45°C	65°C	36.093134	27,706
Airborne Inhabited Cargo	55°C	75°C	31.033319	32,223
Airborne Inhabited Fighter	55°C	75°C	41.003970	24,388
Airborne Rotary Wing	55°C	75°C	86.423756	11,571
Space Flight	30°C	50°C	1.951222	512,499

A.4 Levels

Table A-3 Levels Available

XVB603	Level 1	Level 2
Low temperature	0 °C	-20 °C
High temperature (See WARNING below regarding high temperatures)	55 °C	65 °C
Front panel	YES	YES
Conformal coating		YES
Lithium battery	YES	YES

TIP

Refer to Appendix F, “Processor Speed and Temperature” for more information on High Temperature.

WARNING

The ambient high temperature is dependent on the CPU that is used, the air flow, and other conditions. See Section A.8, "Environmental Compliance" for more details.

A.5 Power Consumption

The following table displays the power consumption of the XVB603.

For measurement purposes, the XVB603 board is mounted on a VME backplane. During measurement, the power consumption of the backplane, keyboard, and the hard disk drive are deducted from the results. The values measured are typical.

The Xeon mobile processor is available in the following CPU option version:

- Quad Core (Xeon) 8 MByte Cache, up to 3.0 GHz

Table A-4 CPU Power Consumption

Processor	Memory	VME Peak Power (5V)
2.2 GHz Xeon Idle	16 GByte	5.8A
2.2 GHz Xeon Test	16 GByte	7.0A
3.0 GHz Xeon Idle	16 GByte	7.8A
3.0 GHz Xeon Test	16 GByte	10.8A

NOTES

Test conditions: T=25 °C, UEFI - defaults, Operating System = Windows 10 64-bit SP1 with Power Management - default, Test Software = Burn-In Pro V 7.1 running 2D video (70%), 3D video (70%), memory (70%), Disk (70%), Ethernet (70%) and CPU (100%).

For every enabled PMC bridge (when adding PMC cards), add 0.45A in addition to the PMC current requirement.

For keyboard, mouse, etc., add 0.1A (typical) to the +5V current

USB connector provides fused VCC voltage (+5V). The total current drawn from this source may not exceed 1.0A.

A.6 Onboard Lithium Battery

An onboard battery (130mAh) supplies the XVB603 RTC. The estimated battery lifetime depends on temperature and power status. See the table below for battery life at non-operating mode (XVB603 power off, RTC supplied by battery) and operating mode (XVB603 power on, RTC supplied by power rail). The XVB603 RTC has a current consumption of 6µA (board non-operating).

A.6.1 Battery Lifetime

The battery lifetime varies with the temperature range.

Table A-5 Battery Lifetime

Mode	Temperature Range	Typical Lifetime in Years
Non-operating	+10 °C to +85 °C	3.5
Non-operating	-10 °C to +10 °C	2.5
Non-operating	< -10 °C	2.0
Operating	-20 °C to +65 °C	10.0

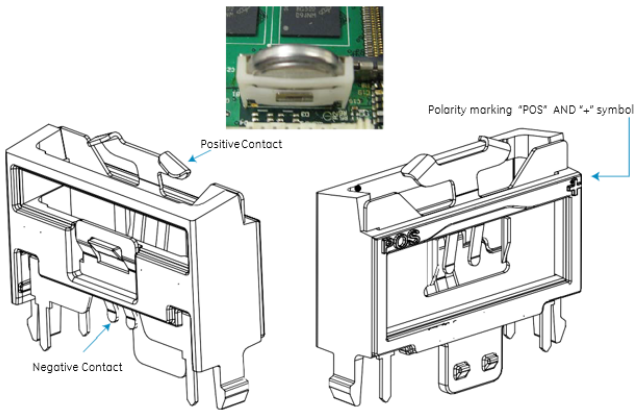
NOTE

When the battery is installed on a non-operating XVB603, the storage temperature range of the board changes from (-50 to +100 °C) to (-40 to +85 °C). See Table A-7.

A.6.2 Battery Removal/Replacement

- Switch off power to unit
- Locate the battery on the computer

Figure A-1 Battery Removal/Replacement



Removal

1. Apply pressure to the bottom of the battery on the solder side of the board. This pushes the battery up allowing more of it to be exposed on the component side of the board.
2. The battery can then be grasped at the top and removed from the socket.

Replacement

A new battery can be installed by sliding it into the holder. Make sure to observe correct polarity.

1. Observe the proper polarity (+) (-).
2. Push the new battery down into the socket until the battery protrudes slightly through the board and the top retaining clips snap into place.

A.7 External Battery Input (+5VSTDBY)

Pin +5VSTDBY located at the VME connector P1 pin B31 can optionally supply current to the RTC and the IPMI controller while the XVB603 is in non-operating mode.

Without battery and without this +5VSTDBY supply voltage, the Real Time Clock oscillator must be started at each power up. The duration increases when operating at lower temperatures and can be up to around 30 seconds (at -40 °C). This delay is below one second at normal ambient temperatures.

It is recommended to use an external supply voltage to this battery input to avoid the power-on oscillator start time and to preserve the date and time information.

The optional +5VSTDBY also supplies the IPMI controller while the XVB603 is in non-operating mode. See the following table for +5VSTDBY current consumption.

Table A-6 +5VSTDBY Current Consumption

+5VSTDBY	RTC	IPMI
XVB603 operating mode	0mA	0mA
XVB603 non-operating mode	2mA	85mA

A.8 Environmental Compliance

Ambient temperatures and humidity values for the XVB603.

Table A-7 Environmental Compliance for Levels 1, 2

Environment	Level 1	Level 2
Cooling Method	Convection	Convection
Conformal Coating	Optional	Standard
High/Low Temperature Operational	0 to +55 °C 300 ft/min airflow	-20 to +65 °C 300 ft/min airflow
Storage Temperature[a]	-50 to +100 °C	-50 to +100 °C
Random Vibration	0.002g^2/Hz 10-2000 Hz random 2g sinusoidal, 5-500 Hz	0.002g^2/Hz 10-2000 Hz random 2g sinusoidal, 5-500 Hz
Shock	20g, peak sawtooth 11ms duration	20g, peak sawtooth 11ms duration
Humidity	Up to 95% RH Non-condensing	Up to 95% RH Non-Condensing varying temperature 10 cycles, 240 hours

[a] Limited to -40 to +85 °C (rather than -50 to +100 °C) if the lithium battery or M.2 is installed.

NOTES

Processor performance and temperature are inter-dependent. For a given temperature, a maximum speed is achievable, and conversely for a given processor speed, a maximum temperature is achievable. Refer to Appendix F, “Processor Speed and Temperature” for more information on Maximum Operating Temperature.

A.9 Electrical Characteristics

The XVB603 requires a supply voltage of +5V. +12V and -12V are only required if needed on the PMC slot. The table below shows voltages with maximum current restrictions due to layout restrictions or fusing:

Table A-8 Supply Voltages

Name	Voltage	Imax	Description
+12V	+12V	0.5A	Supply for PMC-Module
-12V	-12V	0.2A	Supply for PMC-Module
USB_VCC	5V	2.0A	Supply for front panel USB
VTM+3.3V	3.3V	0.5A	Supply for transition module logic

A.9.1 Supply Voltage Range

The following ranges are defined by the VME64 specification ANSI/VITA 1-1994 for VME64 and ANSI/VITA 1.1-1997 for VME64 Extensions. The voltages must be measured at the backplane.

Table A-9 Supply Voltage Range

Supply	Voltage and Tolerance
+5V	5.0V +0.250V / -0.125V
+5V STDBY	5.0V +0.250V / -0.125V
+12V	12.0V +0.60V / -0.36V

A.9.2 GPIO 0...7

The general purpose I/O pins can be used as inputs, with the following signal levels:

Table A-10 GPIO IN Signal Levels

Level	Voltage
Low	-0.3V ... +0.8V
High	+2.0V ... +3.75V (Absolute Max Rating)

When used as outputs (open drain), the following signal levels are supplied:

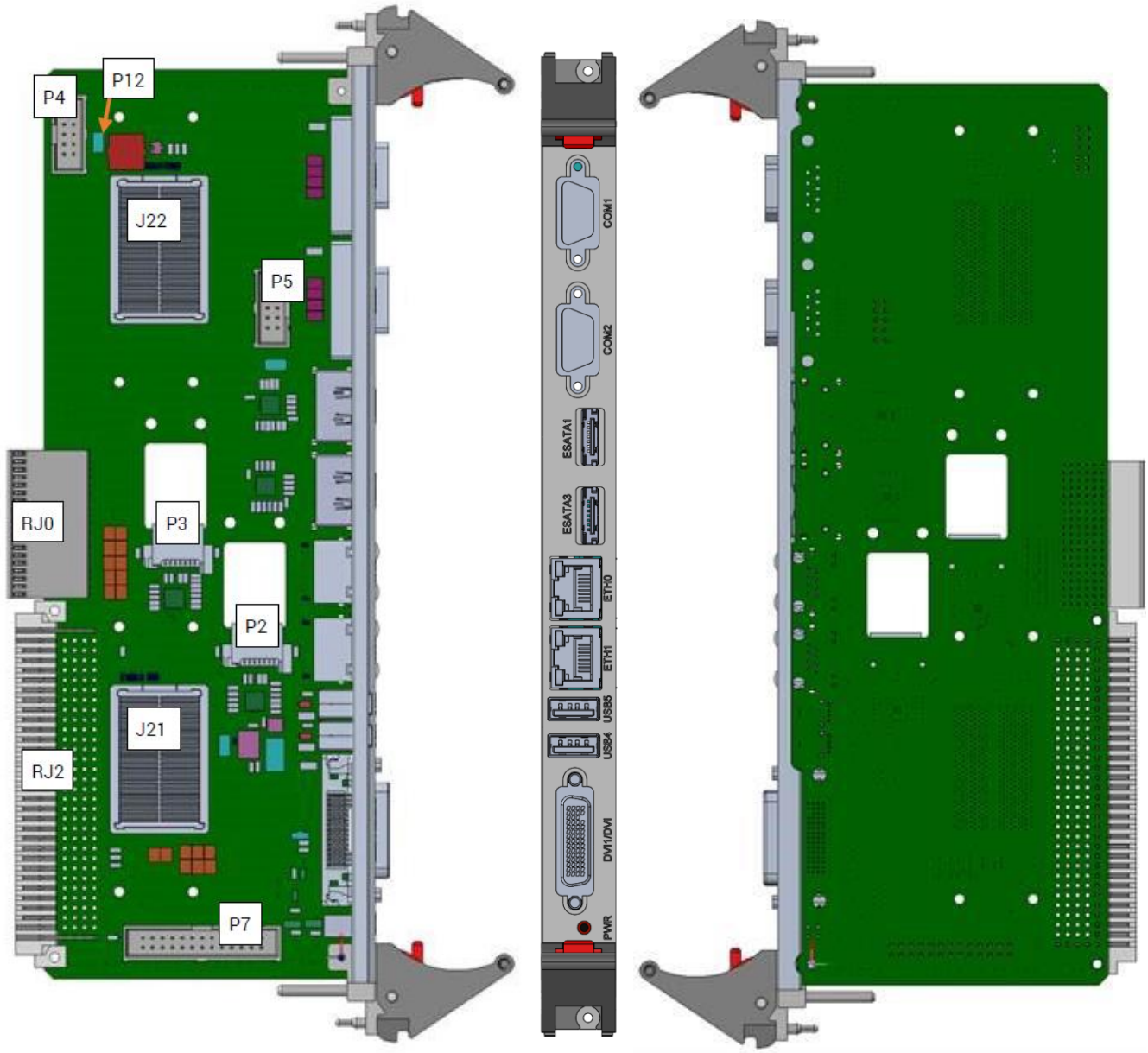
Table A-11 GPIO OUT Signal Levels

Level	Voltage
Low	+0.4V at 6mA sinking
High	10kΩ Pull-up

B • VTM29 Rear Transition Module

This section describes the VTM29 Rear Transition Module (RTM), compatible with the XVB603 and used for easy connection of I/O signals to standard connectors.

Figure B-1 VTM29 Rear Transition Module



B.1 Front Panel I/O Connections

- 2x Gigabit Ethernet ports
- 2x SATA (Gen 2) ports
- 2x USB 2.0 ports
- 2x Serial ports
- DVI-D connector
- Power button

B.2 Top Assembly I/O Connections

- 2x MEZZIO (PMC/XMC) connectors
- 2x SATA connectors
- COM2 header
- GPIO header
- Write Protect header

NOTES

Multiple connections to the RTM are option-dependent. For details, reference the VTM29 manual, document number 522-9300800716-000, at the link below.

LINK

https://www.abaco.com/download/vtm29-hardware-reference-manual

C • UEFI Setup Utility

This appendix gives a brief description of the setup options in the system UEFI firmware. Due to the custom nature of Abaco's SBCs, your UEFI firmware options may vary from the options discussed in this appendix.

To access the Boot Device Selection screen, press the F7 key at the beginning of boot. To access the setup screens, press the F2 or DEL key at the beginning of boot.

C.1 Boot Device Selection Menu

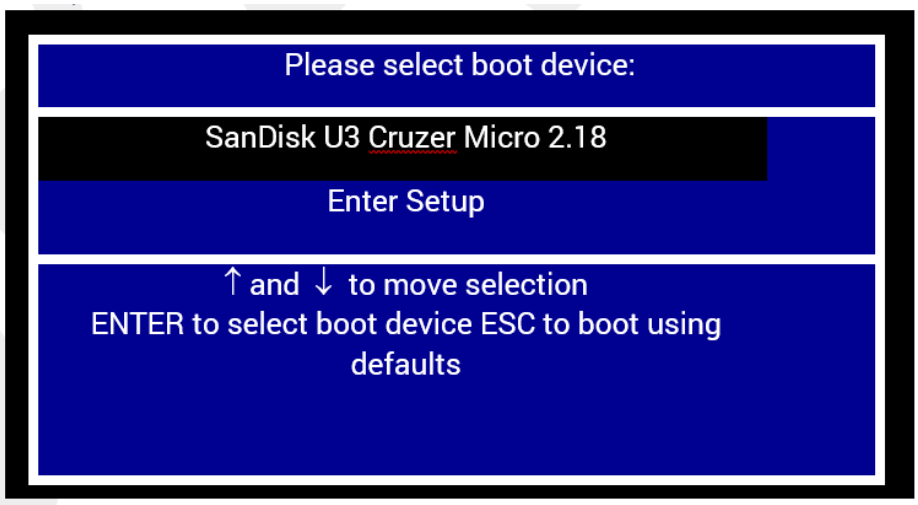
The XVB603 has a Boot Device Selection menu enabling the user to select a drive device to boot from. This feature is useful when installing from a bootable disk. For example, when installing an operating system from a CD, enter the Boot Device Selection menu and use the arrows keys to highlight ATAPI CD-ROM Drive. Press ENTER to continue with system boot.

This feature is accessed by pressing the F7 key at the very beginning of the boot cycle. The selection made from this screen applies to the current boot only and will not be used during the next bootup of the system.

If you have trouble accessing this feature, disable the "Fast Boot" mode in the **Boot** menu of the UEFI (See Figure C-17). Exit, saving changes, and retry accessing the Boot Device Selection menu.

If you do not see your device as expected, see Section C.4.2, "CSM Configuration". CSM Support may need to be Enabled, especially if booting from a legacy operating system, such as DOS.

Figure C-1 Boot Device Selection Menu



C.2 Understanding the Menu Screen Format

The Aptio Setup Utility screen has three main areas. The left frame displays the options that can be configured. The top-right frame gives a brief description of the highlighted option on the left side of the screen. The bottom-right frame shows how to maneuver though the selections and shortcut keys for common actions, such as "F4: Save & Exit".

CAUTION

"**F3: Optimized Defaults**" in the bottom-right side of the screen, will remove any custom settings in ***all*** menus and will restore ***all*** defaults.

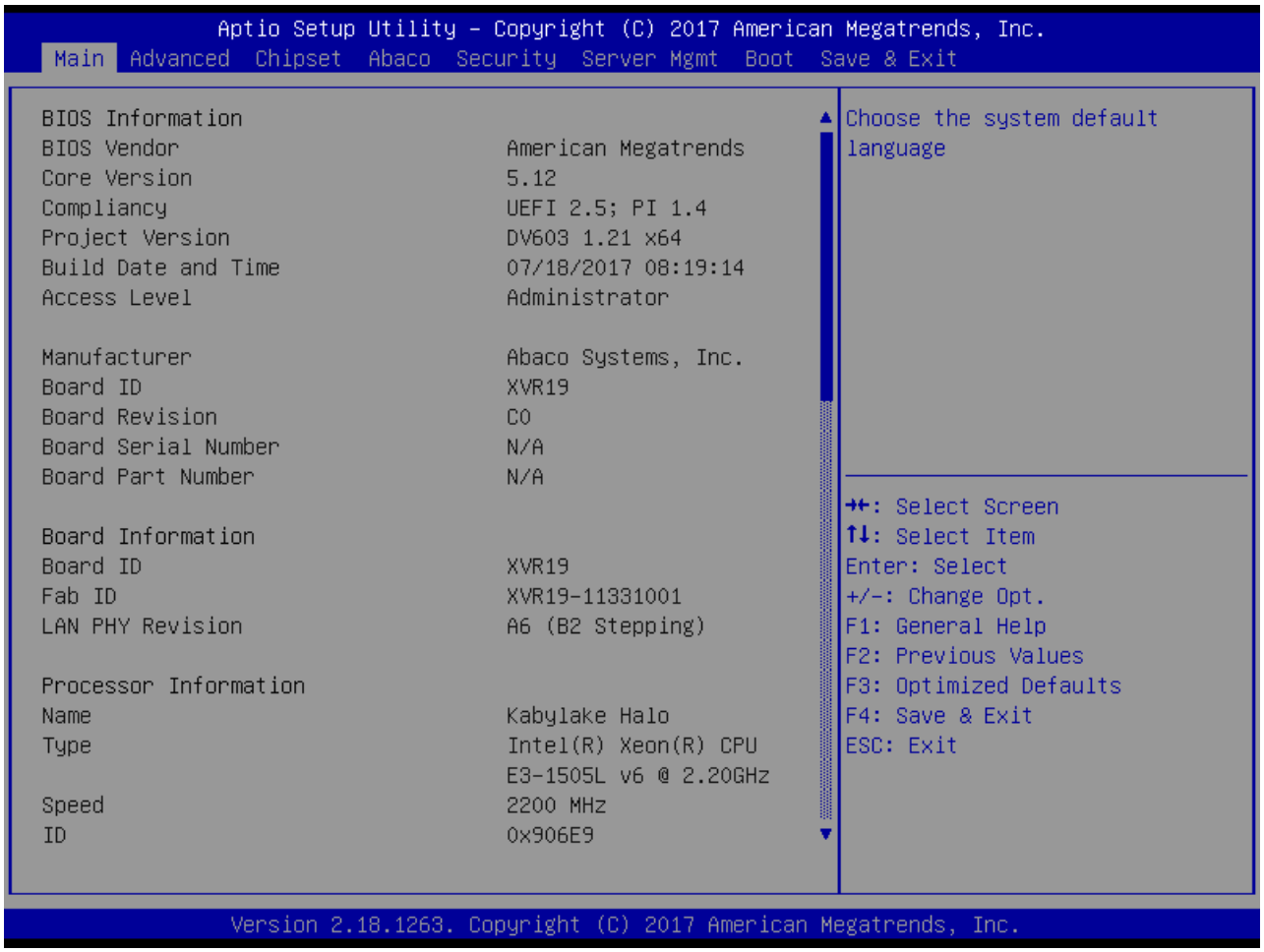
C.3 Main Setup Menu

The **Main** menu reports the UEFI firmware revision and allows the user to set the "System Language", "System Date" and "System Time". Use the left and right arrow keys to select other screens.

NOTE

Below is a sample of the Main screen. The information displayed on your screen will reflect your actual system.

Figure C-2 UEFI Main Menu



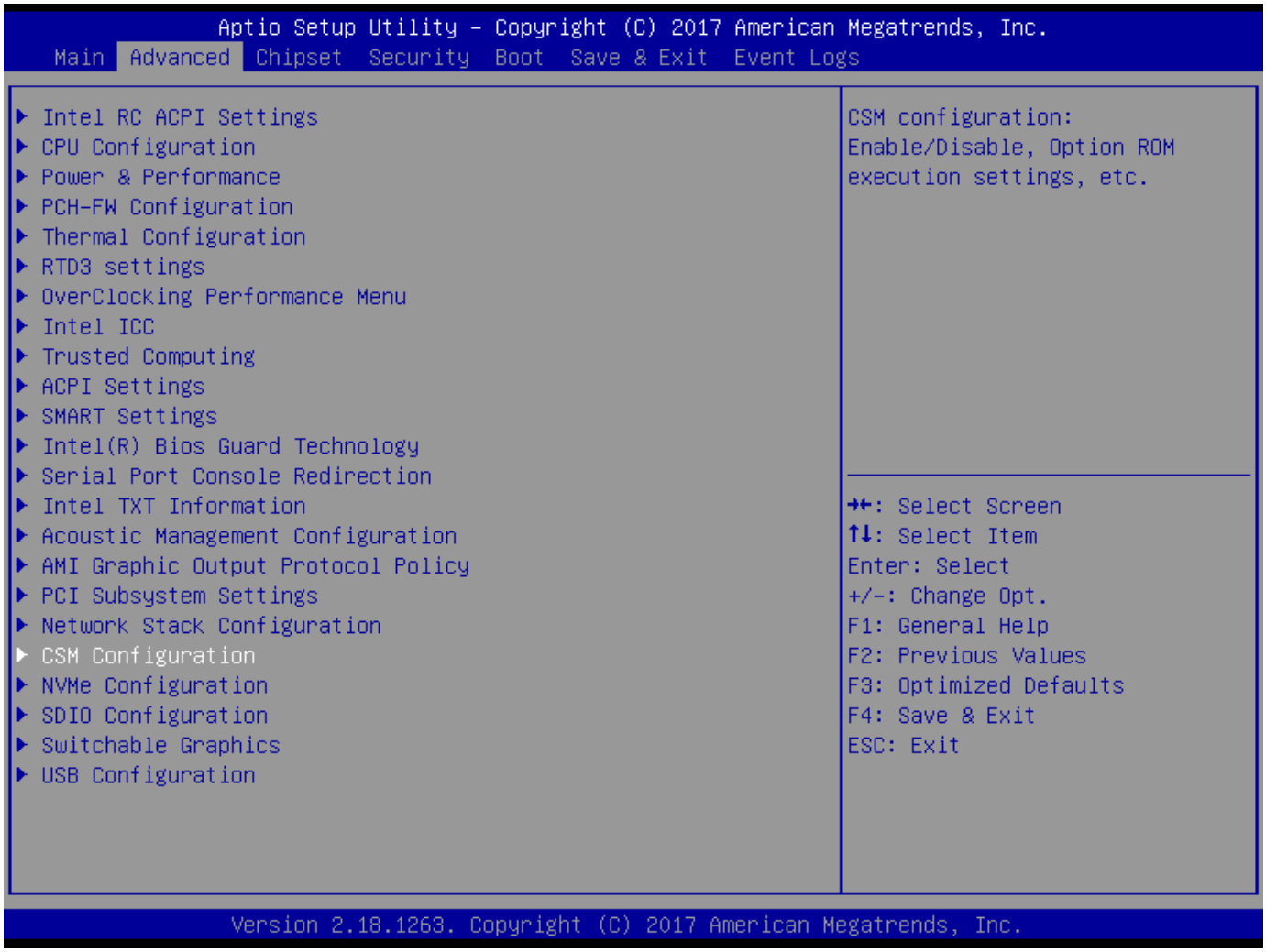
C.4 Advanced Setup Menu

The **Advanced** setup menu allows the user to configure areas such as thermal settings, some CPU settings and USB. The "CSM (Compatibility Support Module) Configuration" is also accessed from this menu. See "Section C.4.2, "CSM Configuration" for setup details.

CAUTION

Changes in this screen can cause the system to malfunction. If problems are noted after changes have been made, reboot the system and access the UEFI firmware. From the Save & Exit menu select '`Restore Defaults`' and reboot the system. If the system failure prevents access to the UEFI firmware screens, refer to Section 3.3.1, "Clear CMOS/RTC/Password" for instructions on clearing the CMOS.

Figure C-3 UEFI Advanced Setup Menu



NOTE

Options shown may not be available on your system.

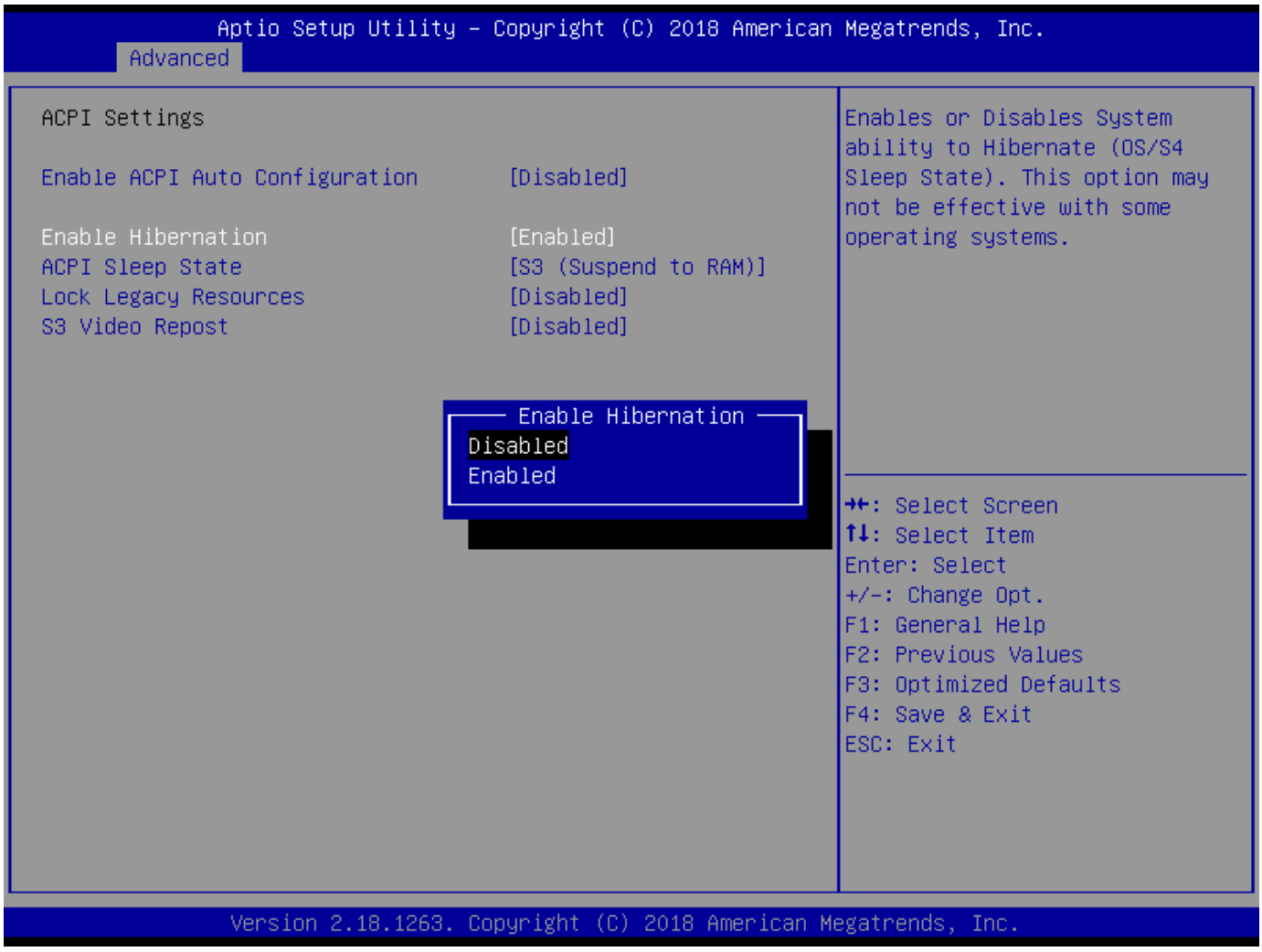
C.4.1 ACPI Settings

The **ACPI Settings** menu allows the user to enable or disable sleep states **S3** (standby) and **S4** (hibernate).

NOTE

The VME specification does not support power-controlled states such as S3 and S4.

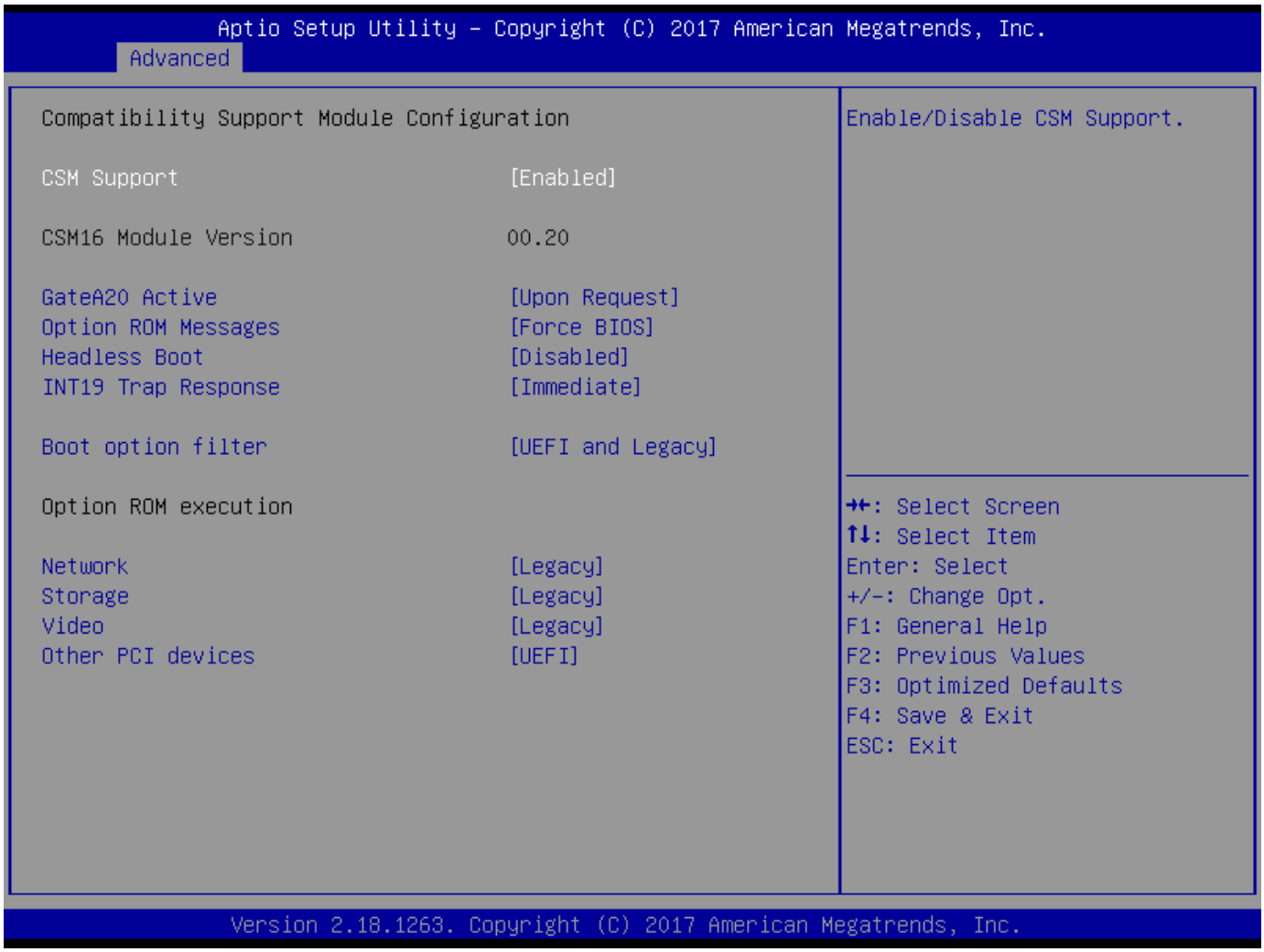
Figure C-4 ACPI Settings Menu



C.4.2 CSM Configuration

The Compatibility Support Module (**CSM**) must be enabled to allow booting from legacy operating systems, such as DOS-based systems, and to use the GbE "Network Boot Configuration" feature under the **Abaco** menu. The "CSM Support" is 'Disabled' by default.

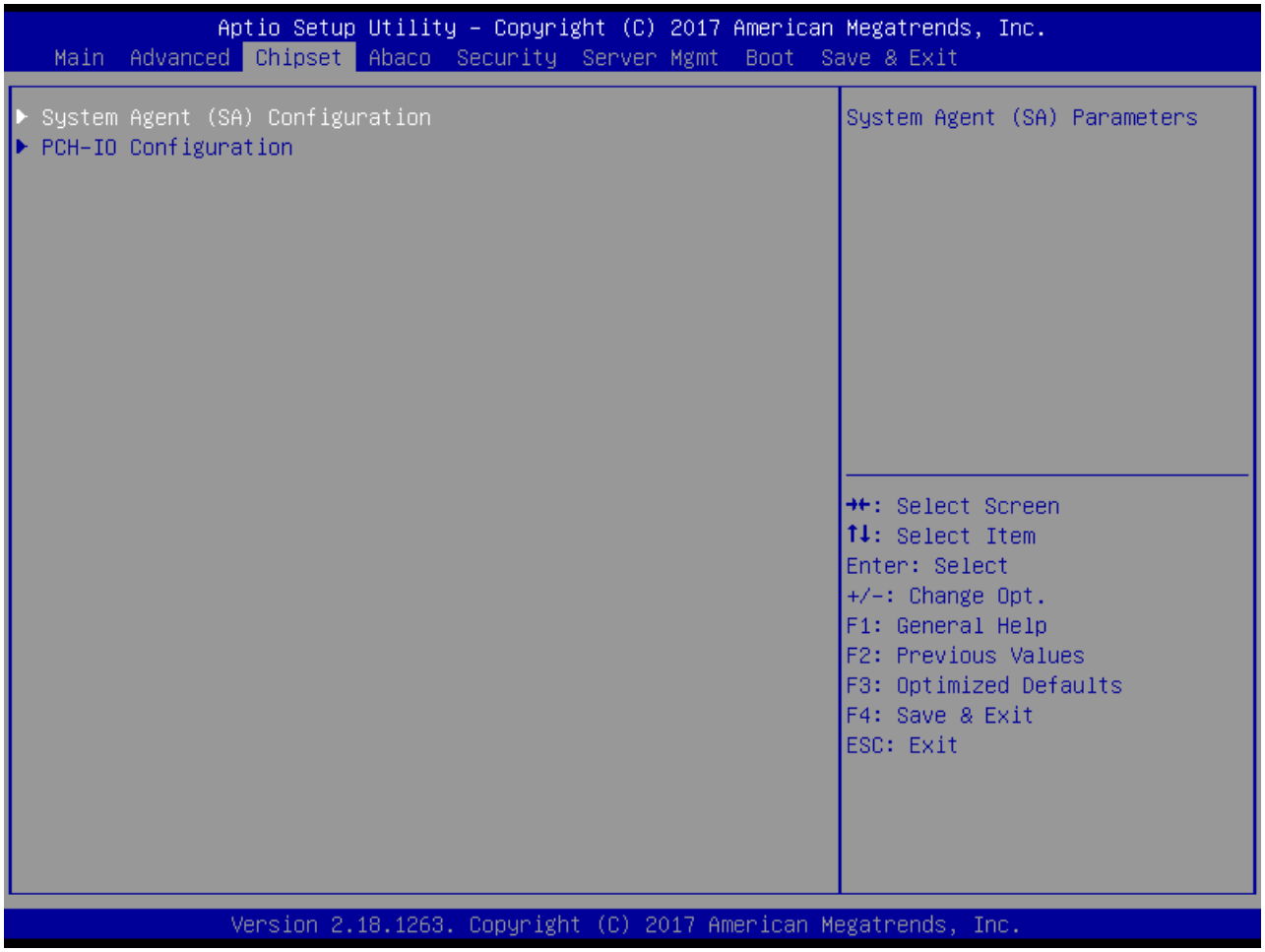
Figure C-5 CSM Configuration Menu



C.5 Chipset Setup Menu

The **Chipset** setup menu allows the user to configure the “System Agent” and “PCH-IO”. The settings for the chipsets are processor-dependent and care must be used when changing settings from the defaults set at the factory.

Figure C-6 UEFI Chipset Setup Menu



C.5.1 PEG Port Configuration

The **PEG Port Configuration** (within the **Chipset – System Agent (SA) Configuration** menu) allows the user to determine the Max Link Speed of each PEG port.
The **Max Link Speed** refers to the speed at which the device communicates with the XVB603.

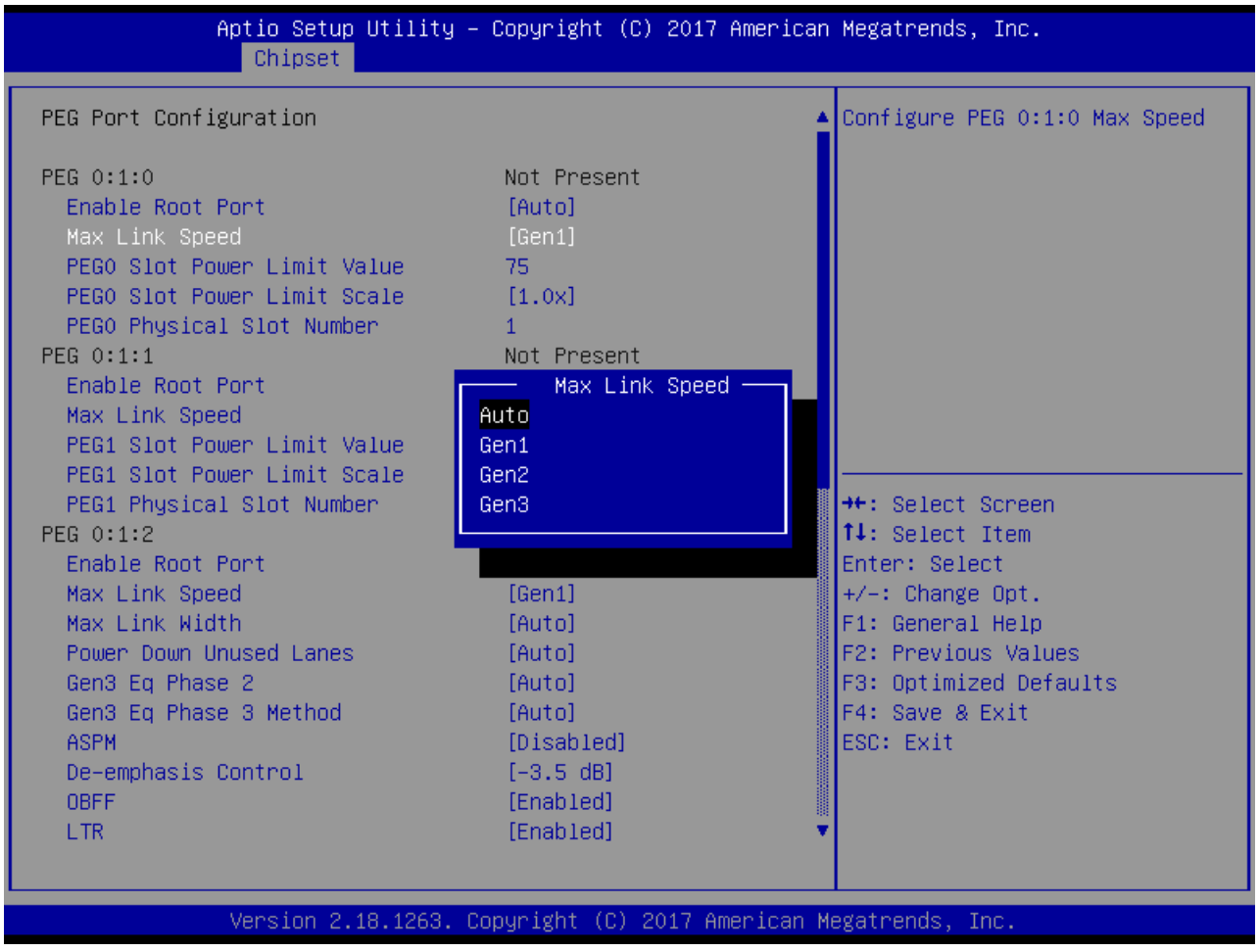
The speed is set separately for each PEG port. The default setting for each is “Gen1”.

PEG 0:1:0 and 0:1:1 ports refer to the XMC devices.
PEG 0:1:2 port refers to a chipset on the board and is only capable of Gen1.

TIP

If the Max Link Speed is set to “Auto” (as shown below), the available speed of the device is used.

Figure C-7 PEG Port Configuration Menu



C.5.2 SATA and RST Configuration

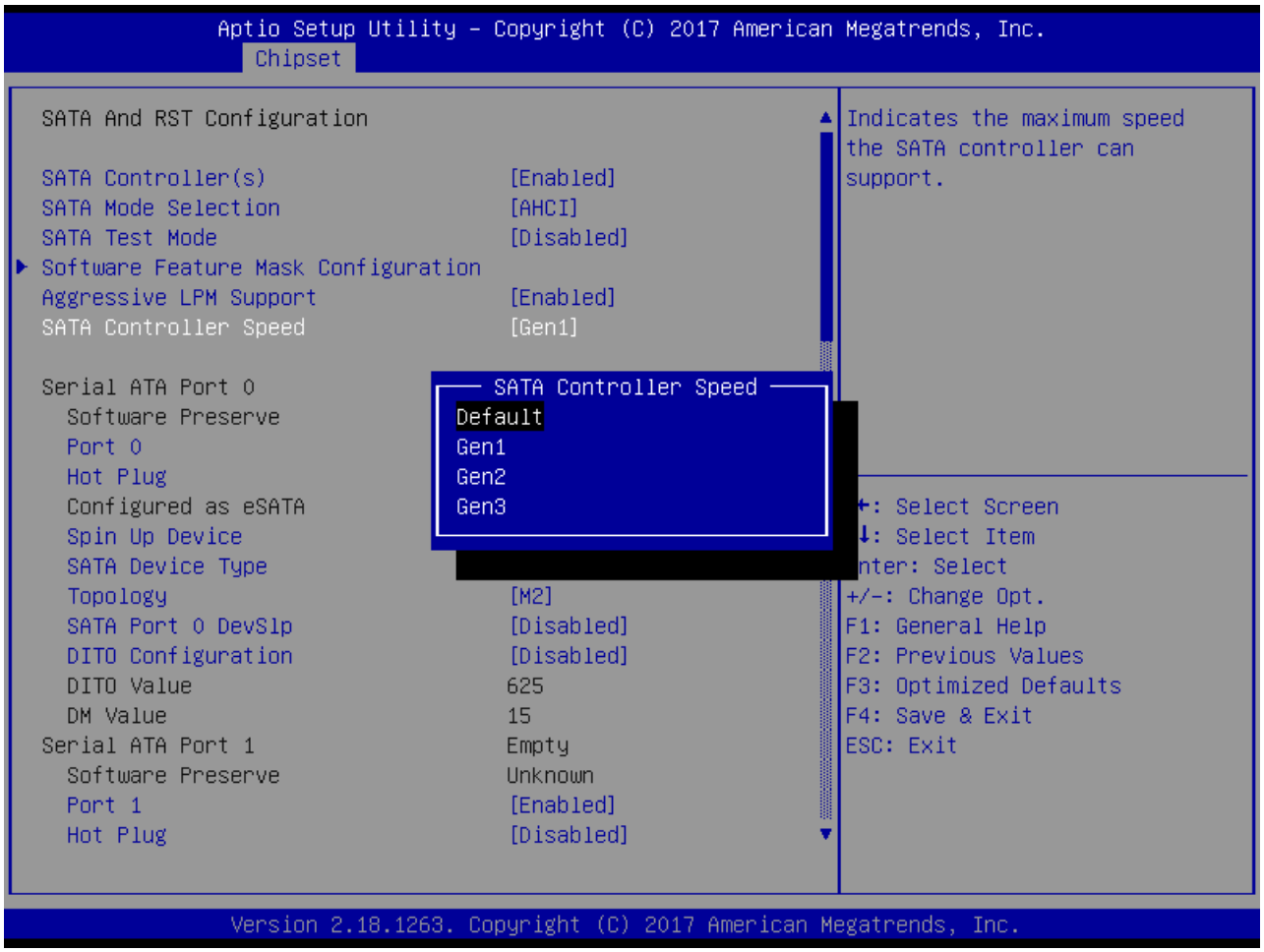
The **SATA and RST Configuration** (within the **Chipset – PCH-IO Configuration** menu) allows the user to determine the SATA Controller Speed for all SATA ports. The **SATA Controller Speed** refers to the maximum speed supported by the SATA controller.

The speed is set once for all SATA ports. The default setting is “Gen1”.

TIP

If the SATA Controller Speed is set to “Default” (as shown below), the available speed of the device is used.

Figure C-8 SATA and RST Configuration Menu



C.6 Abaco Menu

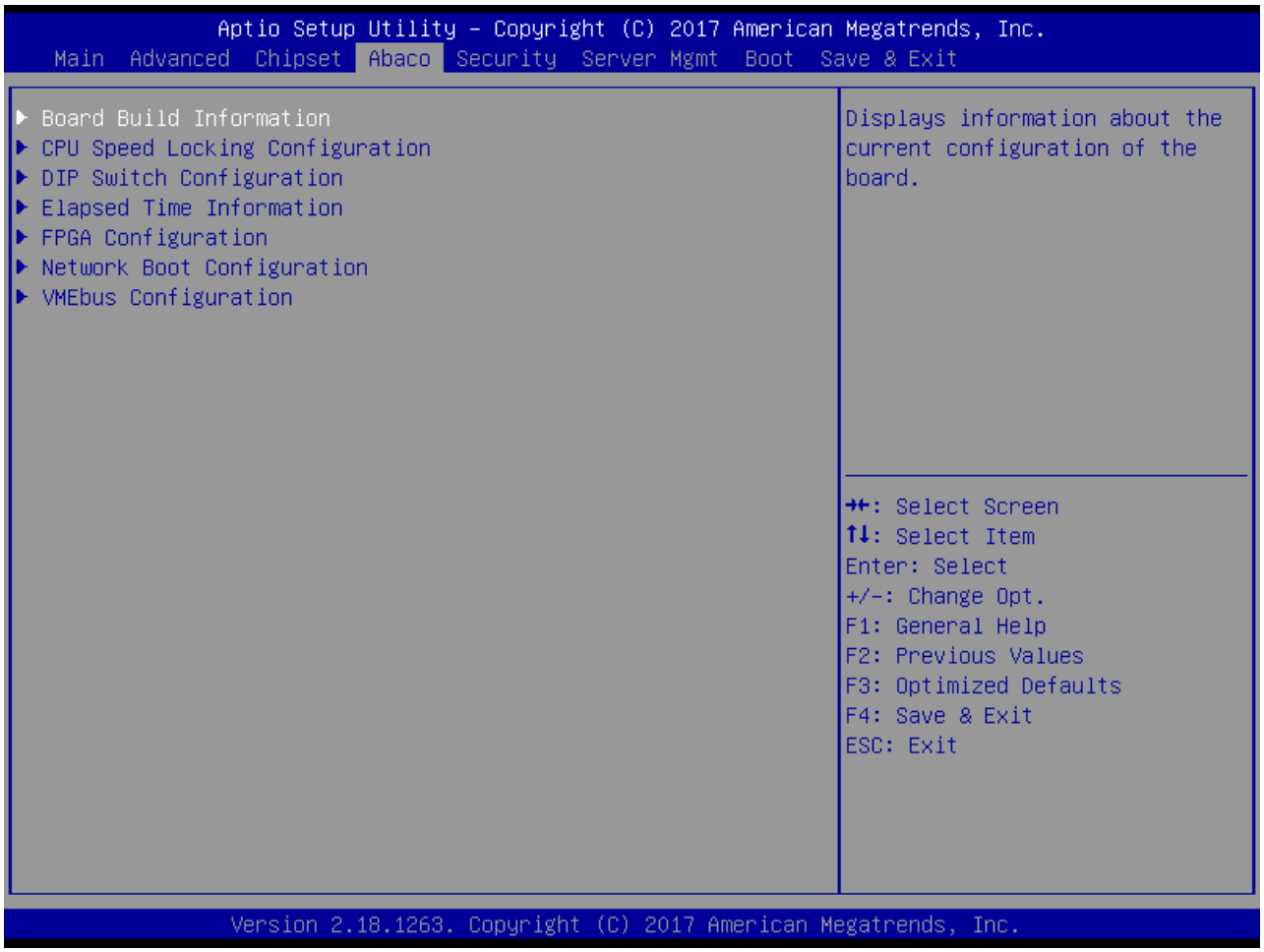
See the following sections for descriptions of the “VMEbus Configuration”, “Network Boot Configuration”, “CPU Speed Locking Configuration”, “Elapsed Time Information” and “DIP Switch Configuration”.

Below is a sample of the **Abaco s**etup screen; the actual options on your system may vary.

CAUTION

Changes in this screen can cause the system to malfunction. If problems are noted after changes have been made, reboot the system and access the UEFI firmware. From the Exit menu select ‘`Restore Defaults`’ and reboot the system. If the system failure prevents access to the UEFI firmware screens, refer to Section 3.3.1, "Clear CMOS/RTC/Password" for instructions on clearing the CMOS.

Figure C-9 Abaco Setup Menu



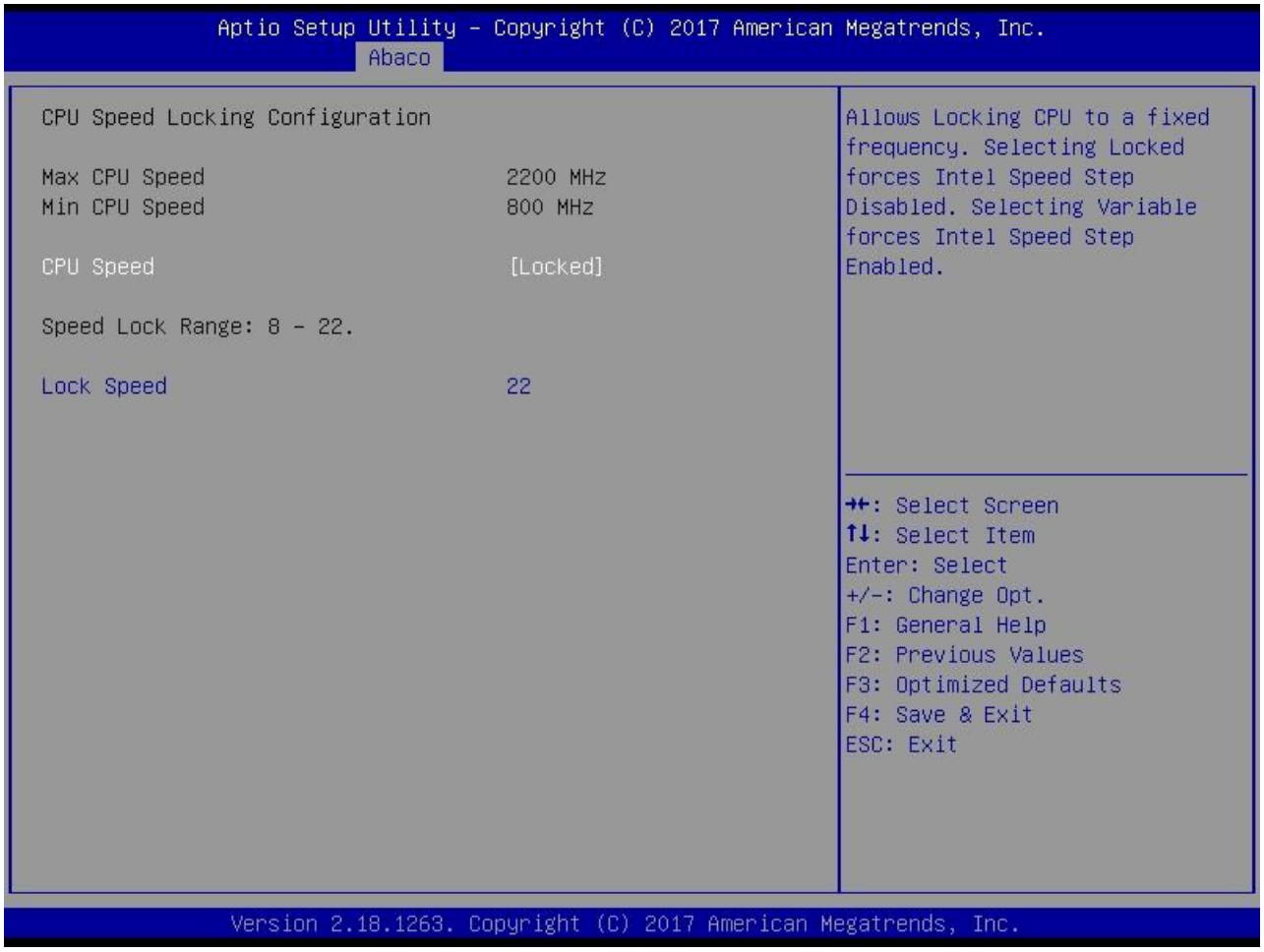
C.6.1 CPU Speed Locking Configuration

The **CPU Speed Locking Configuration** allows the user to set the CPU speed and lock the value or set a variable CPU speed. The allowable range varies depending on the processor. To restore the maximum frequency range to the original range, choose "F3: Optimized Defaults" and reboot the SBC.

CAUTION

"**F3: Optimized Defaults**" in the bottom-right side of the screen, will remove any custom settings in ***all*** menus and will restore ***all*** defaults.

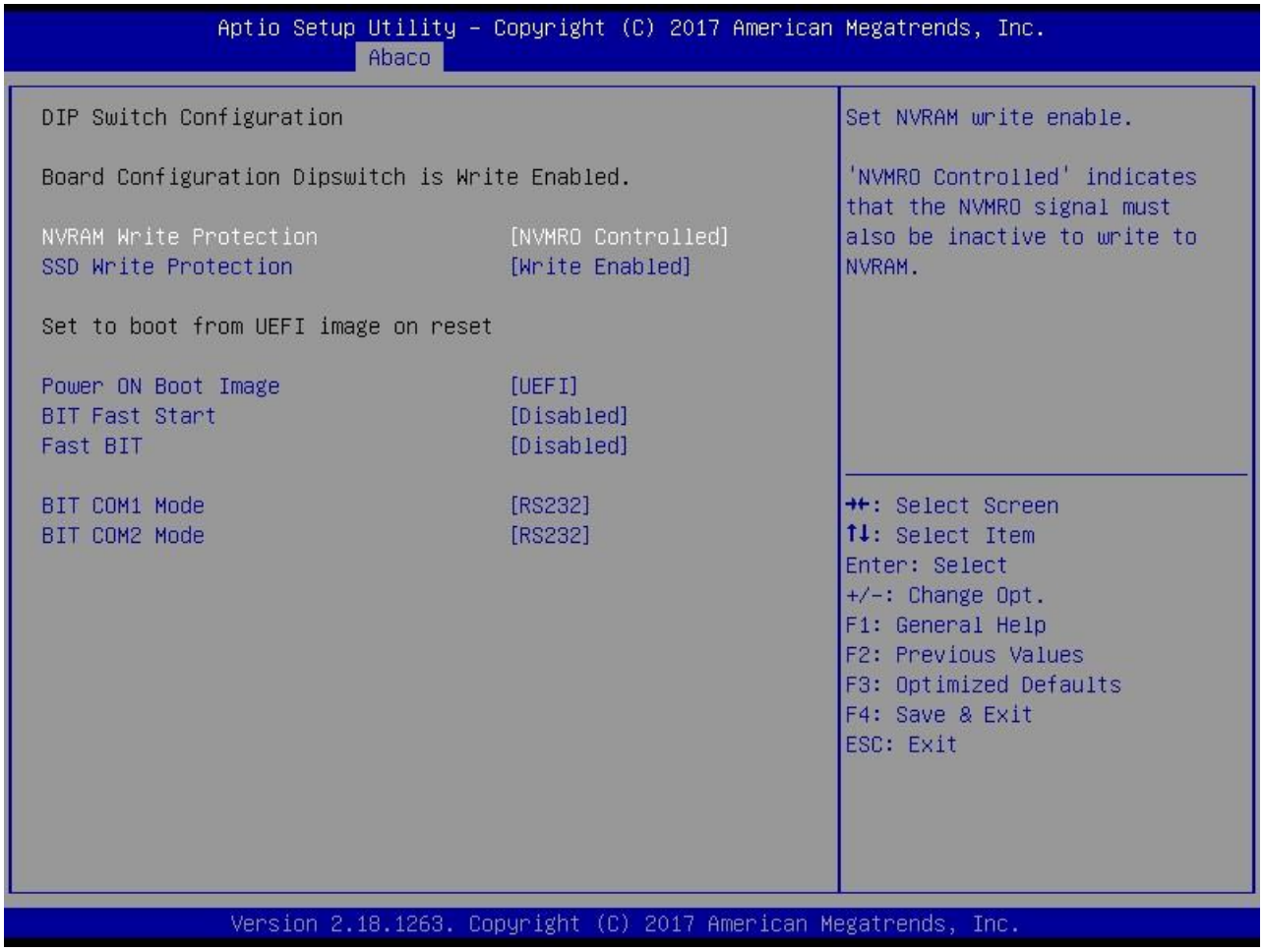
Figure C-10 CPU Speed Locking Configuration Menu



C.6.2 DIP Switch Configuration

The DIP Switch Configuration allows the user the setup “NVRAM Write Protection” and set BIT options, such as “Fast BIT”.

Figure C-11 DIP Switch Configuration Menu



NOTES

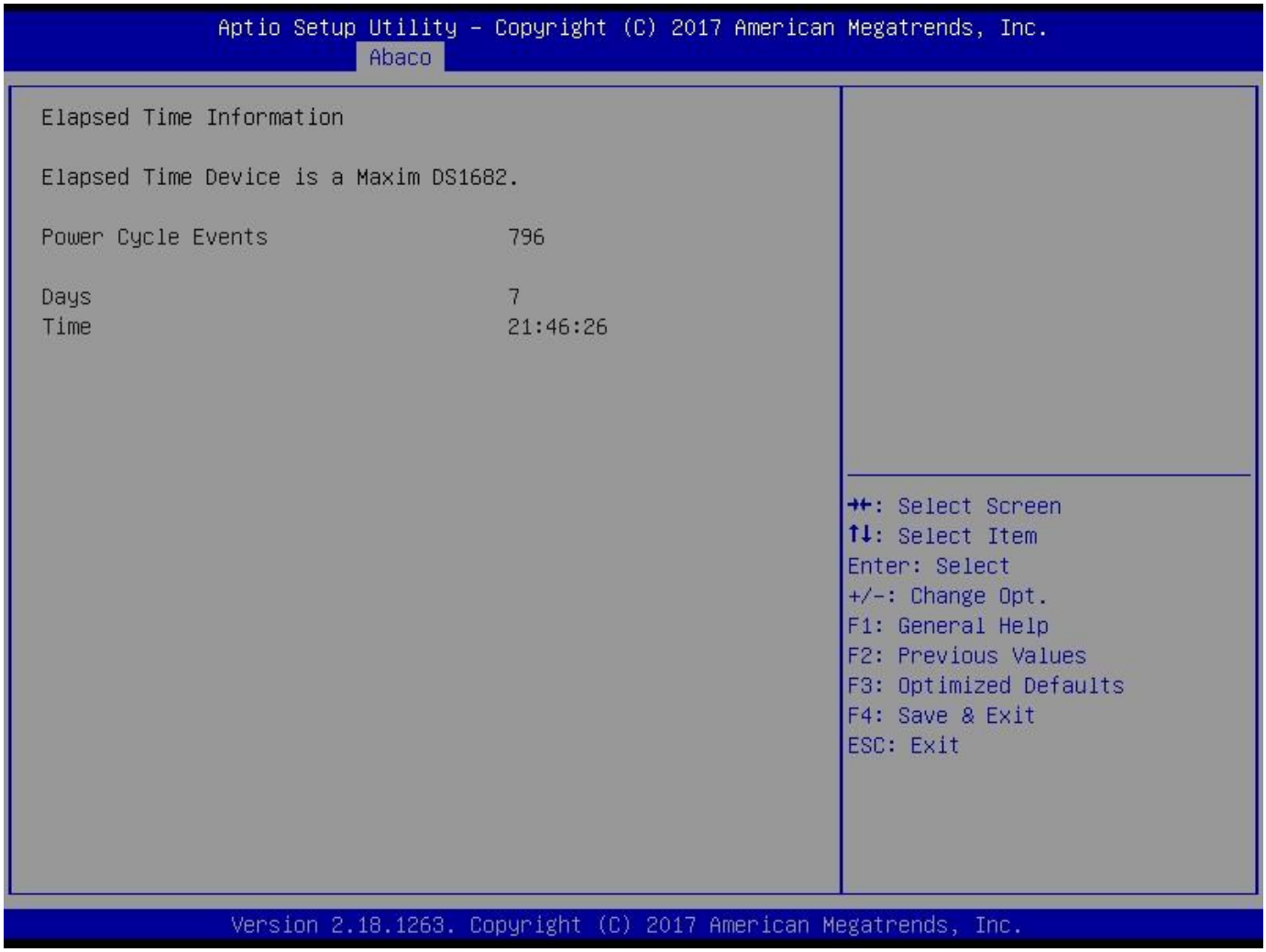
The NVRAM Write Protection setting can only be adjusted when the write-protect jumper (P6) is installed.

Once the “NVMRO Controlled” setting has been saved, the write protection of the NVRAM can be controlled by the NVRAM jumper setting (P6). See Figure 2-1 for the location of P6.

C.6.3 Elapsed Time Information

The **Elapsed Time Information** displays the number of power cycles and runtime.

Figure C-12 Elapsed Time Information Menu



C.6.4 Network Boot Configuration

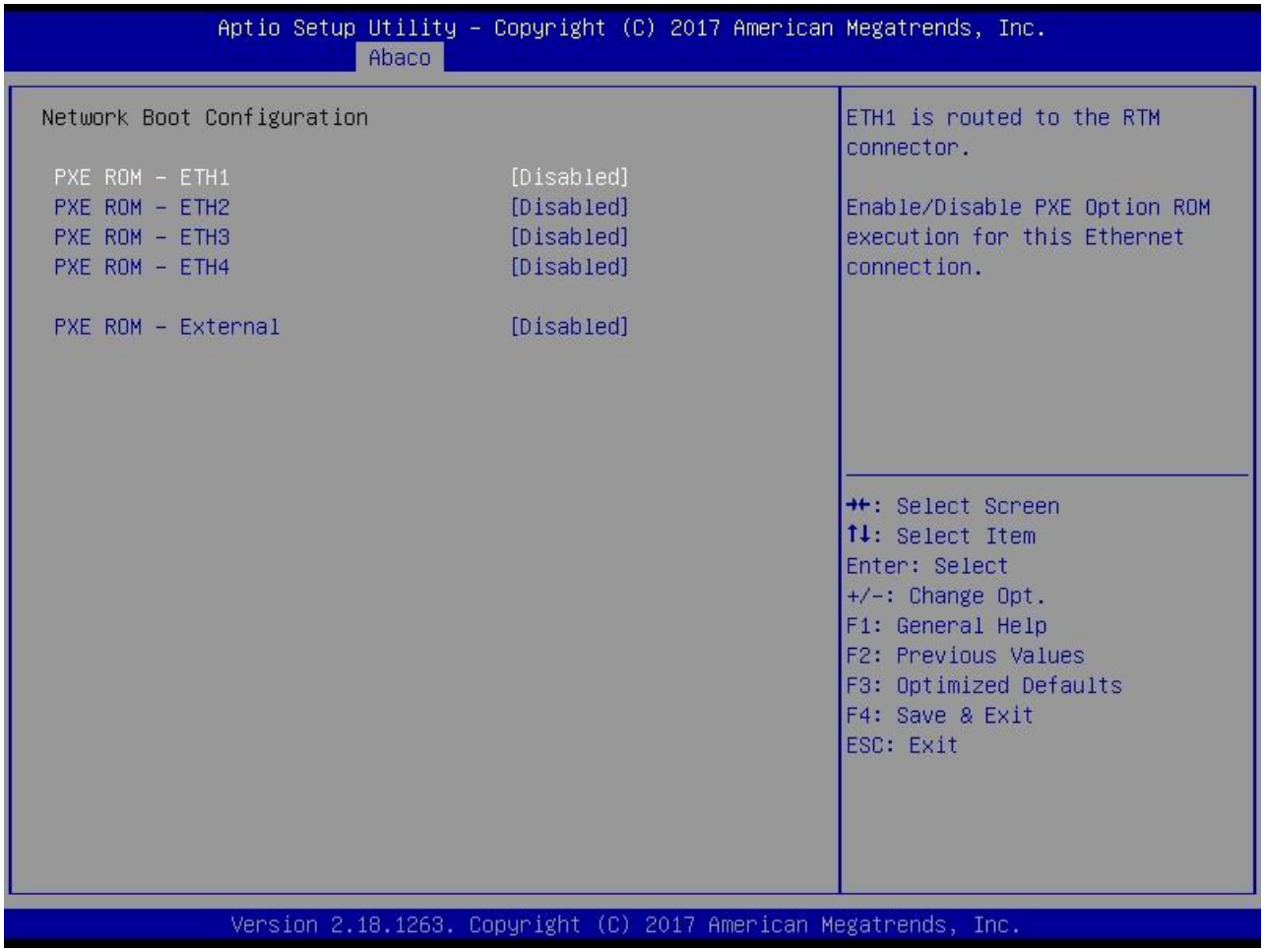
The **Network Boot Configuration** allows the user to enable specific internal and external ethernet ports to boot from a network.

The "PXE ROM – ETHx" selections in the screenshot below define the different internal ethernet ports, with *x* representing the port number. The "PXE ROM – External" selection allows the user to boot from a network with an external PCIe expansion card.

NOTE

Before the **Network Boot Configuration** is setup, the "Network" must be setup within the **Advanced** – **CSM Configuration** menu. See Section C.4.2, "CSM Configuration".

Figure C-13 Network Boot Configuration Menu



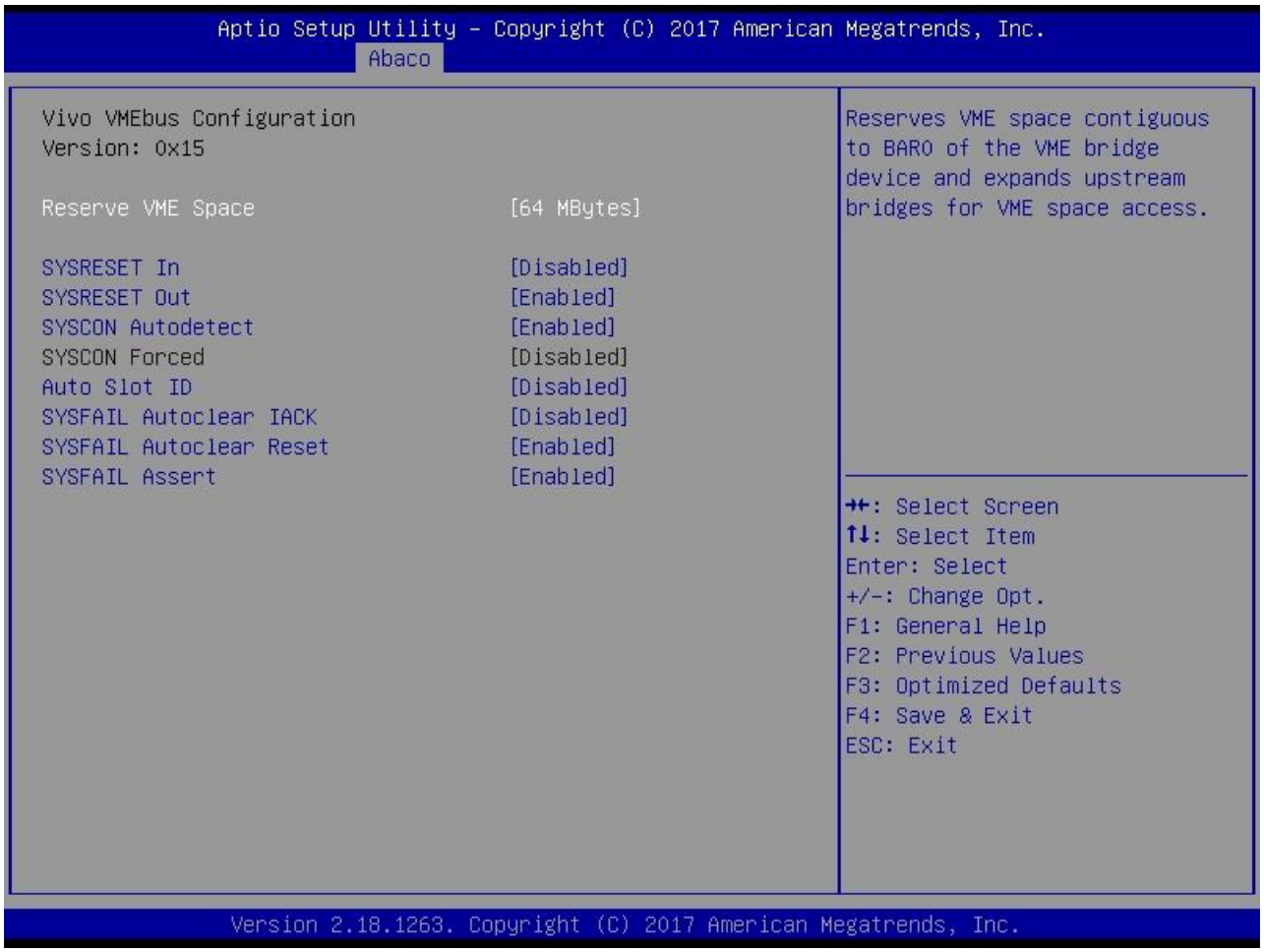
NOTE

The ethernet ports are enumerated during bootup. ETH1 refers to the first ethernet port found; ETH2 refers to the second and so on.

C.6.5 VMEbus Configuration

The VMEbus Configuration setup menu can be used to configure various options for the VMEbus behavior, such as that of the VME/SYSRESET direction. See Section 5.7.3, “VME Non-Volatile Configuration”.

Figure C-14 VMEbus Configuration Menu



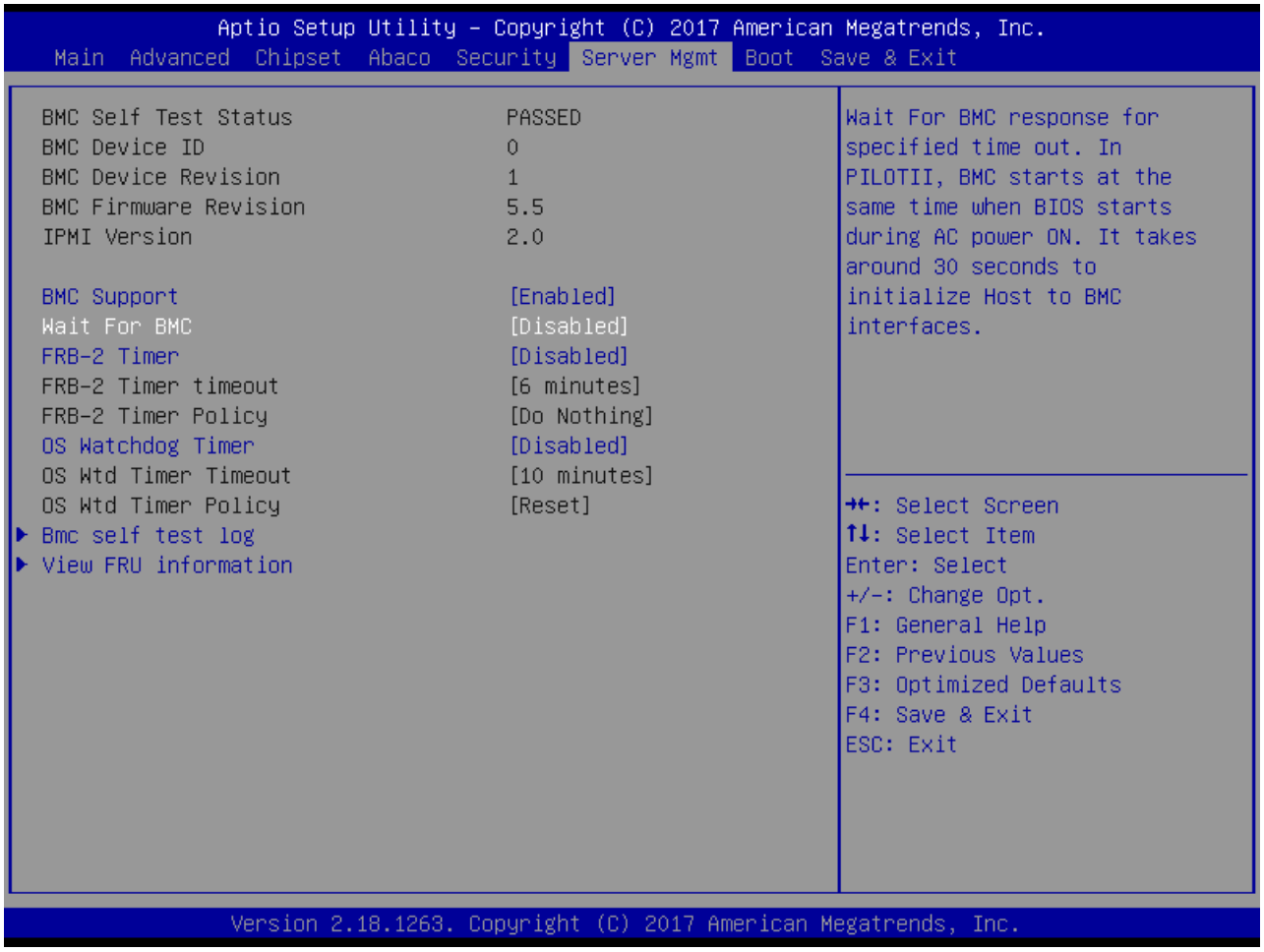
NOTE

The VME configuration (including SYSRESET direction, SYSCON and SYSFAIL) settings may always be modified in the BIOS; however, once they have been modified and saved in the BIOS, a power cycle (reset) **with** P6 **installed** is required before the changes will become active. Once the reset is complete, the jumper may be removed.

C.7 Server Management Menu

The Server Management Menu provides configuration options for watchdog timers and UEFI coordination and communication with the BMC. The menu reports the status of communication with the BMC as may be used to display data collected from the BMC: Self-test information, FRU data.

Figure C-15 UEFI Server Management Setup Menu

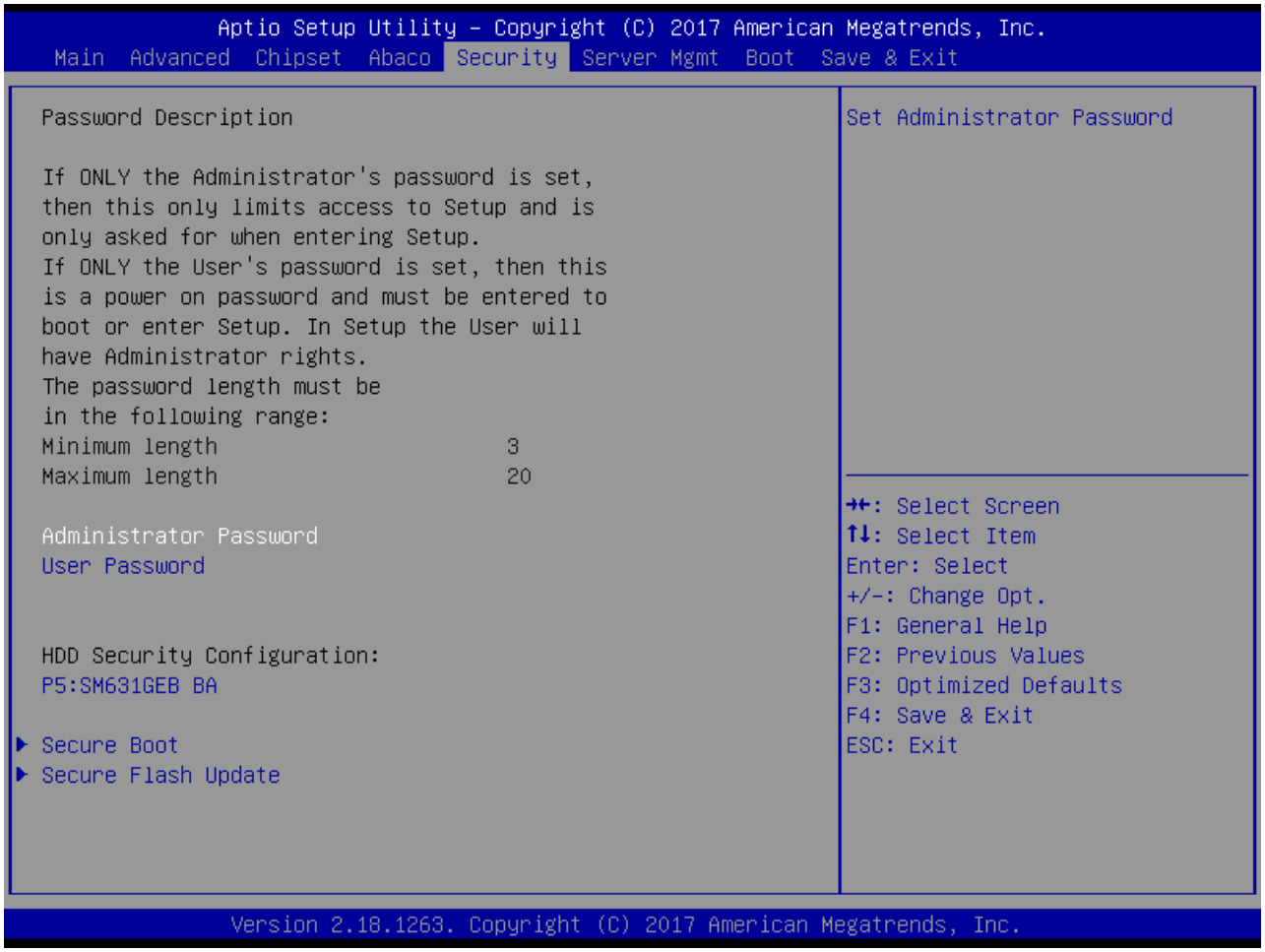


C.8 Security Setup Menu

The **Security** setup provides both an Administrator and a User passwords. If you use both passwords, the Supervisor password must be set first.

The system can be configured so that all users must enter a password every time the system boots or only when setup is executed, using either the Administrator or User password.

Figure C-16 UEFI Security Setup Menu

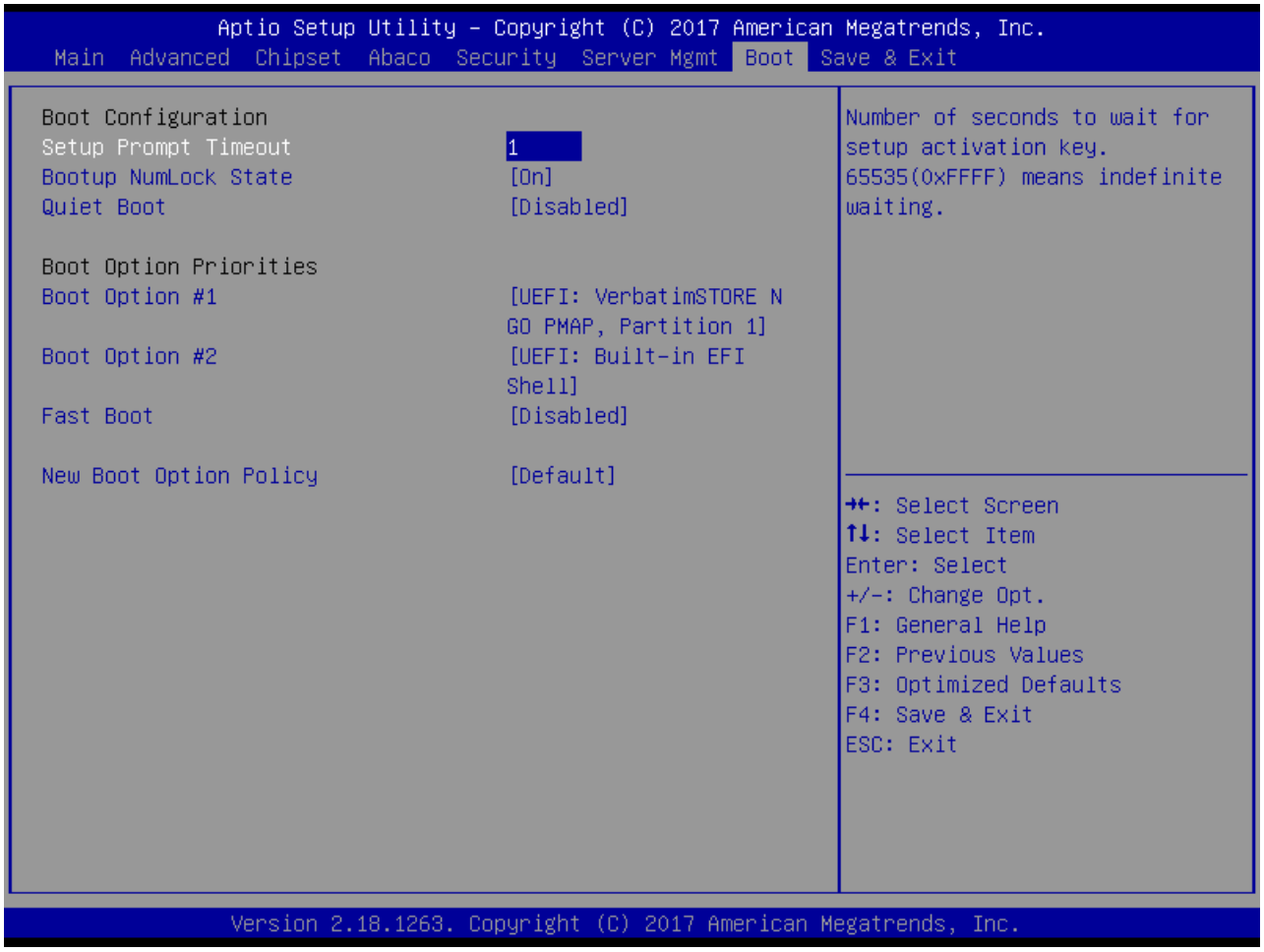


To reset the security in the case of a forgotten password, you must clear the CMOS and reconfigure. Refer to Section 3.3.1, "Clear CMOS/RTC/Password" for instructions on clearing the CMOS.

C.9 Boot Setup Menu

Use the **Boot** Setup menu to set the priority of the boot devices, including booting from a remote network. The devices shown in this menu are the bootable devices detected during POST. If a drive is installed that does not appear, verify the hardware installation.

Figure C-17 UEFI Boot Setup Menu



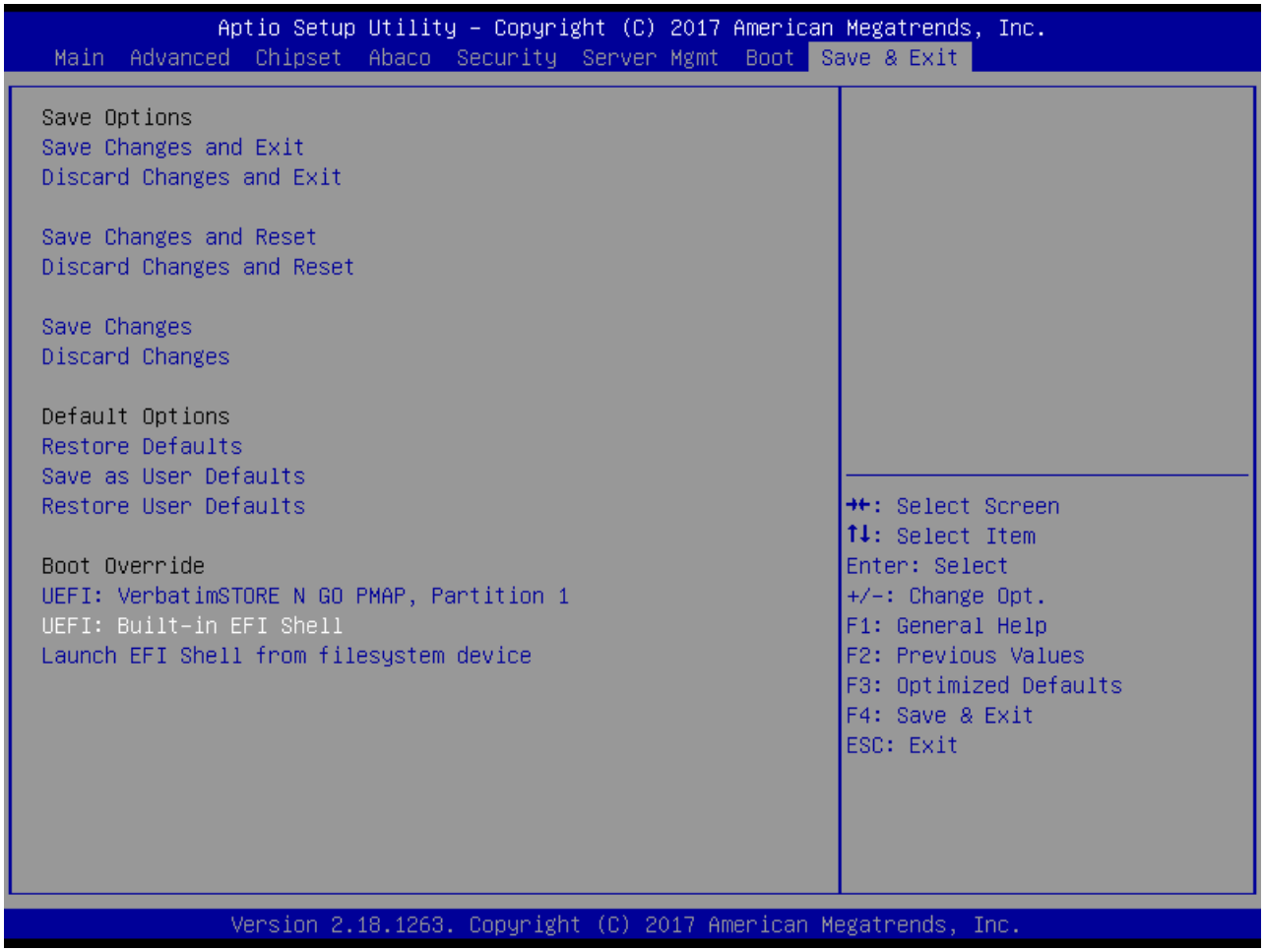
C.10 Save & Exit Menu

Select the **Save & Exit** tab from the setup screen to save changes made within the UEFI setup. “Save Options” will save the changes, keeping the setup utility open. “Save Changes and Exit” will save changes, exit the utility and reboot the system with new changes.

NOTE

Changes can cause the system to malfunction. If problems are noted after changes have been made, reboot the system and access the UEFI setup. From the **Save & Exit** menu select “Restore Defaults” and reboot the system. If the system failure prevents access to the UEFI setup screens, refer to Section 3.3.1, "Clear CMOS/RTC/Password" for instructions on clearing the CMOS.

Figure C-18 UEFI Save & Exit Menu



D • Mezzanine Site

D.1 PMC/XMC Slot

The PCI Mezzanine Card (PMC/XMC) interface is an additional slot for parallel mounted add-on cards. The interface is compliant to the IEEE 1386.1 specification and is based on the electrical and logical layer of the PCI specification. PMC slot is 33/66/133 MHz PCI-X capable.

- The PMC has a 3.3V key mounted for 3.3V compatible PMC cards.

D.1.1 Electrical Characteristics

Table D-1 Electrical Characteristics

Parameter	Comment	Value
5V	Max. current on 5V Pins	1.5A [c]
+12V	Max. current on +12V Pin	0.1A
-12V [a]	Max. current on -12V Pin	0.1A
V(I/O) [b]	Voltage for PCI I/O	3.3V or 5V
P	Max. power consumption total	7.5W

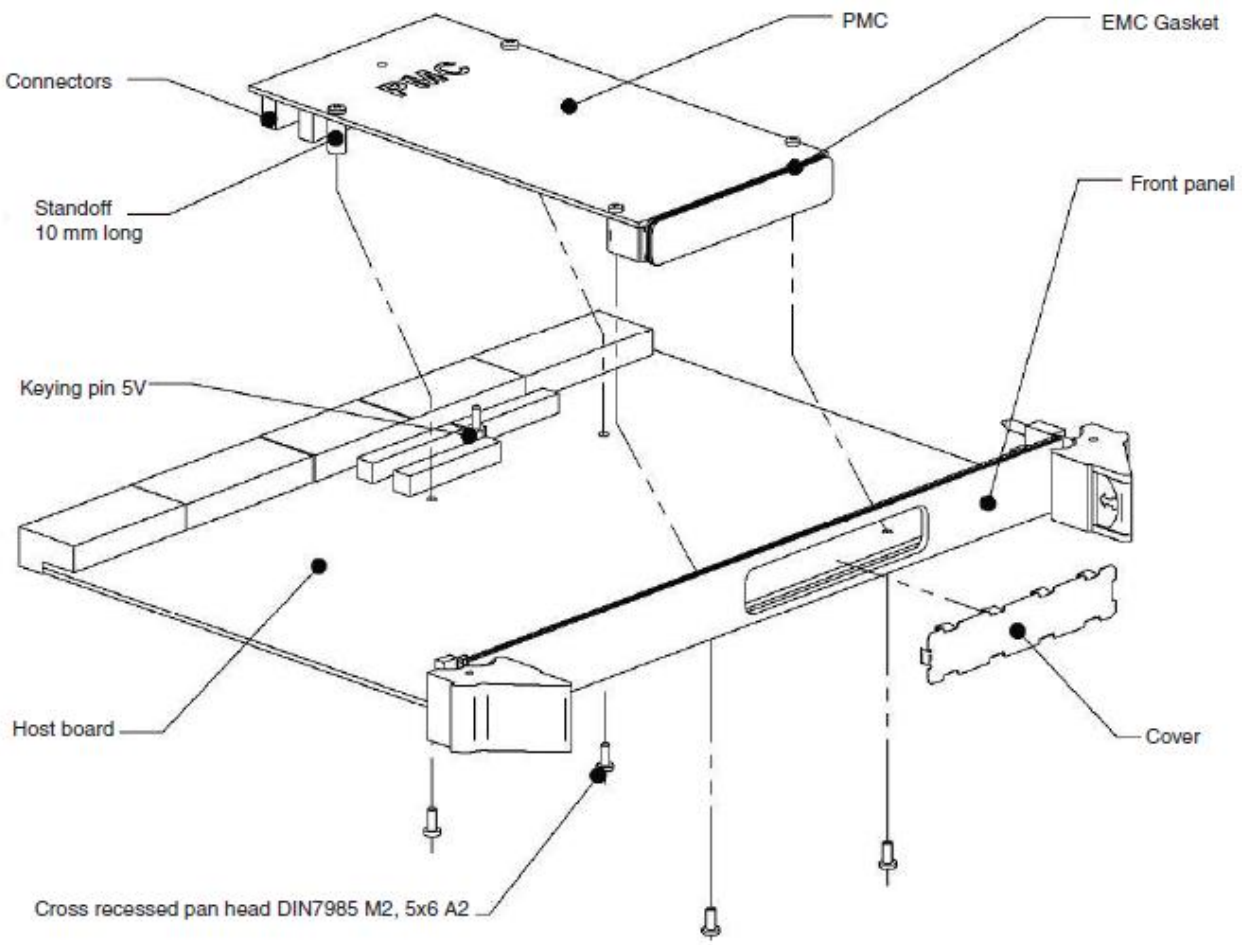
[a] -12V must be connected to the backplane.
[b] The appropriate key must be mounted.
[c] Total power dissipation on 3.3V and 5V rail is 7.5W.

D.1.2 Mounting of PMC or XMC Module

To mount a PMC or an XMC board to the XVB603, follow these steps:

1. Remove XVB603 from system housing.
2. Remove the front panel cover of the PMC/XMC slot.
3. Take the PMC/XMC from inside through the front panel and then press connectors together.
4. Verify correct installation of the EMC gasket.
5. Affix the PMC/XMC onto the host boards with four screws. Screws must be locked with Loctite 243.

Figure D-1 Mounting PMC/XMC Module onto XVB603



NOTE

Aside from the board-to-board mating connectors, the mechanics/hardware are the same for mounting PMC and XMC cards.

E • EXP238 Expansion Board Option

The EXP238 is a PCI Expansion module that extends the PMC- and XMC-capability of the XVB603 SBC (also referred to as the host). The EXP238 is a 6U VMEbus form factor expansion card offering three XMC/PMC expansion sites (0 – 2). Each expansion site provides an opportunity for front I/O. Rear I/O is also supported through PMC site 0 (PMC0), providing 46 lines of rear PMC I/O through the J14 connector.

NOTE

When the XVB603 with EXP238 option is used, the XMC/PMC site on the host board is not available.

The EXP238 implements a PCIe to PCI-X bridge immediately after the connection to the host SBC, ensuring compatibility with PCI loading specifications. The EXP238 also includes a PCIe switch allowing the x8 PCIe lanes from the host to be configured as three x4 PCIe XMC sites.

The initialization firmware or BIOS of the XVB603 will correctly configure the PCIe to PCIX bridge as well as any PMC or XMC devices. Additional interaction with devices on the EXP238 is the responsibility of driver's, specific to the PMC or XMC module installed. Reference Figure E-1 for a functional block diagram of the EXP238.

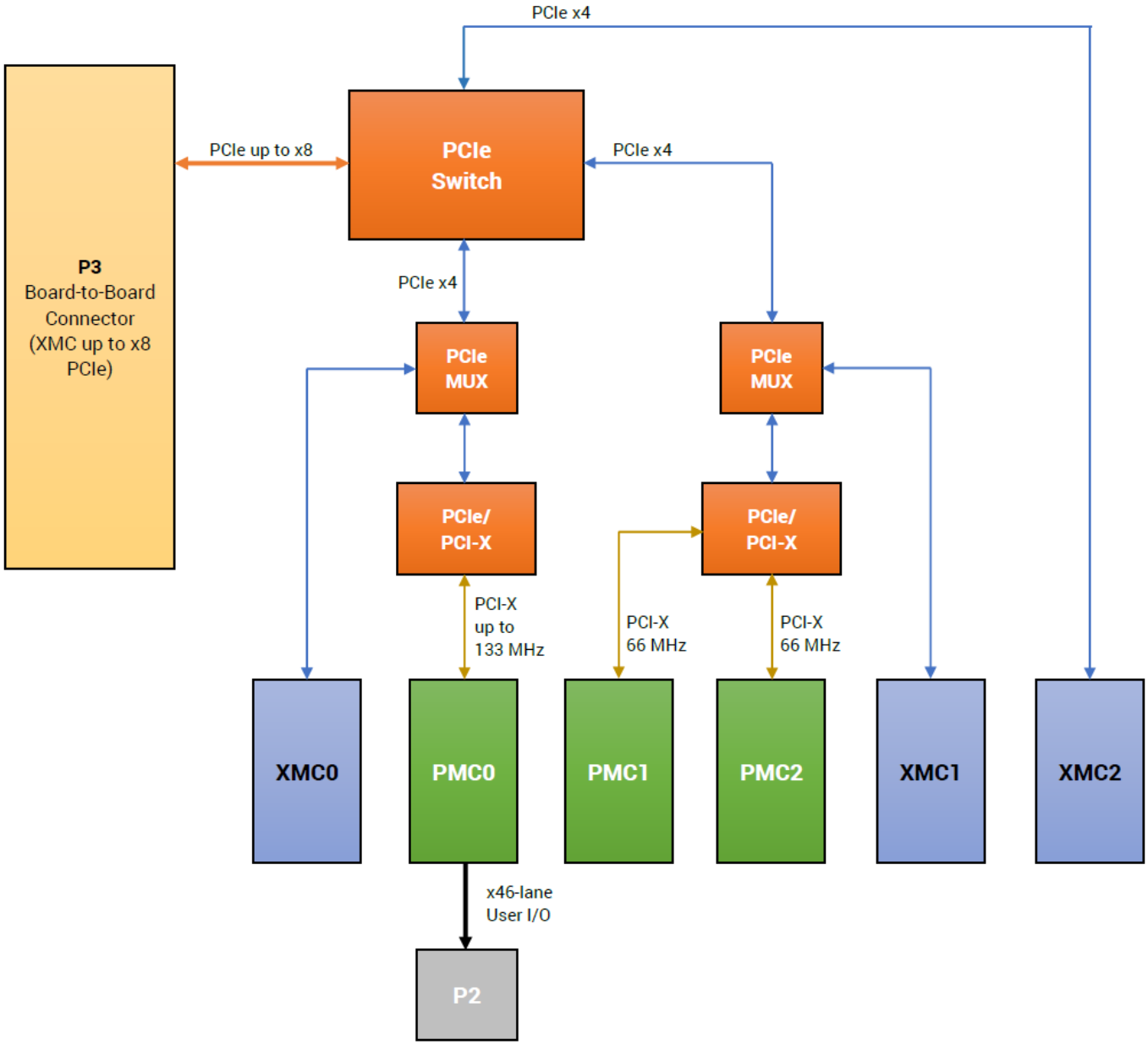
E.1 Features of the EXP238

- 3x XMC/PMC expansion sites via PCIe to the XVB603 through an onboard connector
  - 1x PMC – PCI-X up to 133 MHz (PMC0) (3.3V VIO)
  - 2x PMC – PCI-X up to 66 MHz (PMC1 and PMC2) (3.3V VIO)
  - 3x XMC – x4 PCIe
- VITA 42.3 XMC connector compatible
- VME connection (P1) with depopulated pins for easier insertion and extraction. See Section E.5 for pin assignments.
- Front I/O available on all 3 PMC/XMC sites
- 46-lane Rear I/O available from PMC0 through the VME P2 connector per VITA 35-2000, Single PMC-P4 to VME64 x-P2, rows D, Z
- Card Voltages
  - 3.3V supplied by the EXP238
  - 5V and 12V supplied by the backplane

NOTE

The Default VIO voltages of the PMC sites are 3.3V but may be adjusted to 5V by moving the PMC Keying pins. Contact factory for details.

Figure E-1 EXP238 Functional Block Diagram



E.2 EXP238 Interrupt Mapping

The PCI bus has four interrupt lines: INTA, INTB, INTC, and INTD. The EXP238 routes these interrupts to the host PMC attachment in the following fashion:

Table E-1 PCI Interrupt Mapping

Device	Component	Vendor ID	Device ID	Address Map ID Select	PCI IRQ	Arbitration Request Line
PCIe to PCIe Switch	PLX8725	0x10B5	0x8725	N/A	N/A	N/A
PCIe to PCI-X Bridge	PI7C9X130	0x12D8	0xE130	N/A	N/A	N/A
PMC Site 0	N/A	N/A	N/A	AD24	INTA	REQ0
PMC Site 1	N/A	N/A	N/A	AD24	INTA	REQ0
PMC Site 2	N/A	N/A	N/A	AD25	INTB	REQ2

E.3 Mechanical Construction of XVB603 with EXP238 Installed

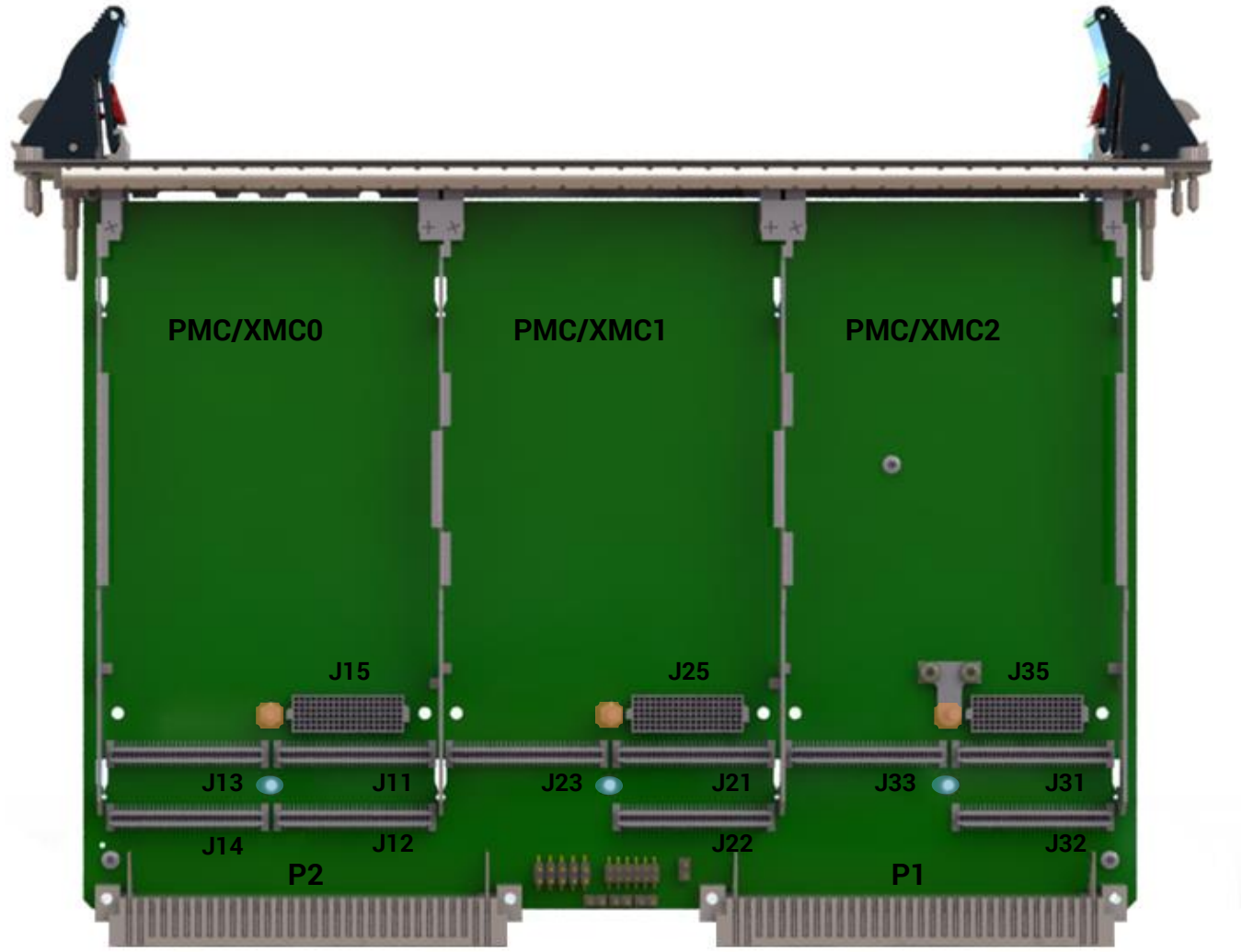
Table E-2 Mechanical Construction with EXP238 Installed

Aspect	Details
Form Factor	6U, dual slot, 8HP
PCB	FR4 Multilayer
Dimensions*	233.35 mm x 178 mm x 40.46 mm
Weight	2.3 lb

* Measured from the backplane connector mounting plane to the front panel face.

E.4 EXP238 Expansion Sites and Connectors

Figure E-2 EXP238 Expansion Sites and Connectors



NOTES

PMC keying pins shown in the figure above (highlighted with) are all used for 3.3V signaling only and set by the factory. If the card(s) needs access to 5V from the backplane, reseat keying pin into 5V keying pin hole (highlighted with).

The hardware for the 3.3V keying pin on PMC/XMC site 2 cannot be refitted in the 5V keying pin nut. If the card being fitted onto site 2 requires 5V, additional hardware will be needed. See Table E-3 for ordering information.

E.5 Adjusting the Keying Pins

The EXP238 is set to 3.3V signaling from the factory. For PMC/XMC sites 0 and 1, the keying pins and washers in the 3.3V locations can be removed and inserted into the 5V locations. See Figure E-2 for the location of the keying pins.

The hardware installed in the 3.3V keying pin location of site 2 cannot be transferred to the 5V location. Extra hardware is needed (provided with the board).

In case extra is needed, the table below provides the ordering details of the keying pin hardware needed to use 5V signaling on PMC/XMC site 2. One of each part is needed. Figure E-3 relates the part numbers to the drawing of the part.

Table E-3 Keying Pin Hardware Details

Vendor Part Number	Vendor and Description	Torque	Comment
BN670 M2.5	Bossard Metric M2.5 Washer, Flat		Washer
MMX1411-M12-F21-M2.5-2	Unicorp M2.5 Male-Male Standoff 5mm Hex Body	2.5 in-lb	Male-male standoff (keying pin)

TIP

The hardware listed for the 5V signaling on site 2 is the same hardware used in sites 0 and 1.

E.5.1 Steps to Adjust the Keying Pins

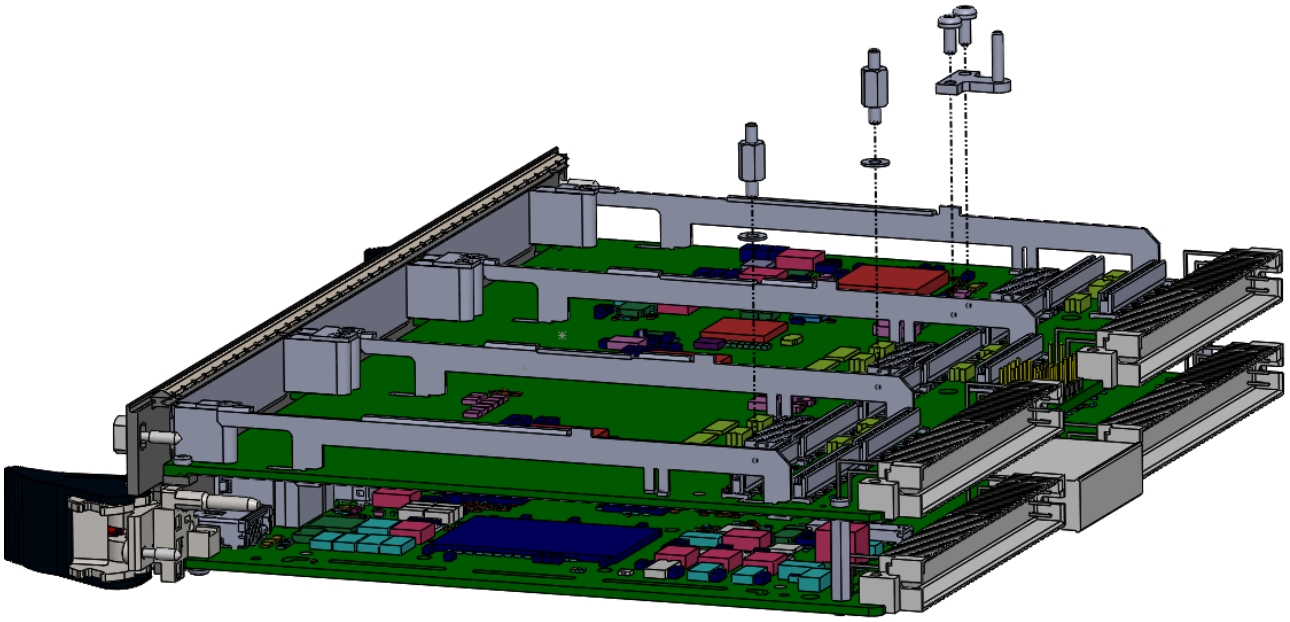
Follow the steps below to adjust the keying pin and change the signaling voltage on the EXP238 PMC/XMC expansion sites.

NOTES

For each PMC/XMC site: Keying pins may not be installed in both the 3.3V and 5V locations at the same time (regardless of whether they physically fit).

1. Remove the keying pin and washer from current location.
2. Re-install into the desired location (washer placed under keying pin) using a torque of 2.5 in-lb.

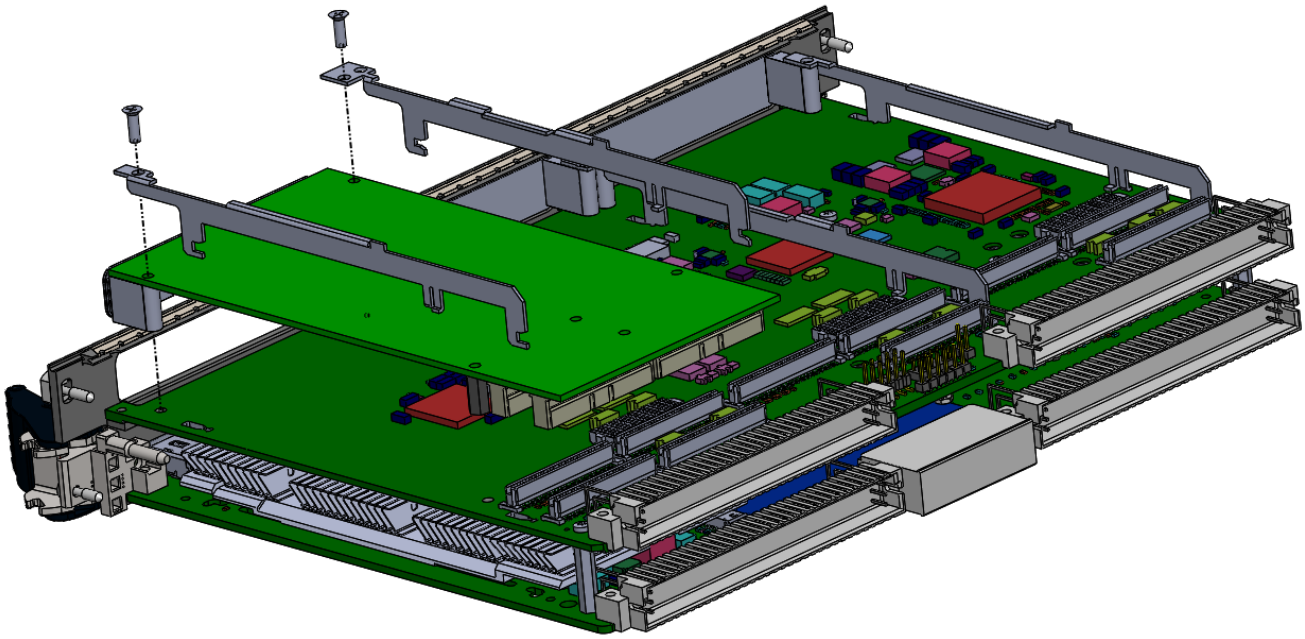
Figure E-3 Adjusting the Keying Pins on the EXP238



E.6 Installation of a PMC/XMC Card on the EXP238 Carrier Board

1. Remove the easy rails from the board
2. Install the PMC/XMC card onto the EXP238 carrier board and push down on all connectors to ensure contact. Refer to the product manual of the PMC/XMC module for configuration and setup.

Figure E-4 Installing PMC/XMC Card onto EXP238



NOTE

Inserting an XMC card into Site 1 disables any PMC connection in Site 2. See the table below for possible site configurations of XMC and PMC cards.

Table E-4 Possible PMC/XMC Site Configurations Available

PMC/XMC Site 0	PMC/XMC Site 1	PMC/XMC Site 2
PMC or XMC	XMC	XMC Only
PMC or XMC	PMC	PMC or XMC

NOTE

One, two or three sites can be populated at the same time. Neither is dependent on another to be functional. Only the configuration of the *type* of card (PMC or XMC) needs to follow the patterns in the table above.

E.7 EXP238 PMC Connectors

The PCI Mezzanine Card (PMC) carries the same signals as the PCI standard; however, the PMC standard uses a completely different form factor. Table E-5 through Table E-9 display the pinouts for the XMC/PMC connectors.

E.7.1 PMC Connectors and Pinouts (J11, J21, J31)

Figure E-5 PMC Connector (J11, J21, J31)

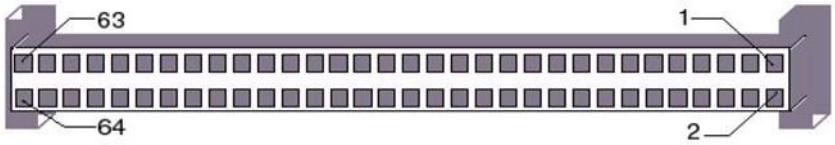


Table E-5 PMC Connector Pinout (J11, J21, J31)

PMC Connector (J11, J21, J31)				PMC Connector (J11, J21, J31)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	JTAG_TCK*	2	-12V	33	FRAME#	34	GND
3	GND	4	INTA#	35	GND	36	IRDY#
5	INTB#	6	INTC#	37	DEVSEL#	38	+5V
7	BMODE1#	8	+5V	39	PCIXCAP	40	LOCK#
9	INTD#	10	N/C	41	SDONE#	42	SBO#
11	GND	12	N/C	43	PAR	44	GND
13	CLK	14	GND	45	VCC_PMC_IO	46	AD[15]
15	GND	16	GNT#	47	AD[12]	48	AD[11]
17	REQ#	18	+5V	49	AD[9]	50	+5V
19	VCC_PMC_IO	20	AD[31]	51	GND	52	CBE[0]#
21	AD[28]	22	AD[27]	53	AD[6]	54	AD[5]
23	AD[25]	24	GND	55	AD[4]	56	GND
25	GND	26	CBE[3]#	57	VCC_PMC_IO	58	AD[3]
27	AD[22]	28	AD[21]	59	AD[2]	60	AD[1]
29	AD[19]	30	+5V	61	AD[0]	62	+5V
31	VCC_PMC_IO	32	AD[17]	63	GND	64	REQ64#

* For factory use only.

E.7.2 PMC Connectors and Pinouts (J12, J22, J32)

Figure E-6 Connector (J12, J22, J32)

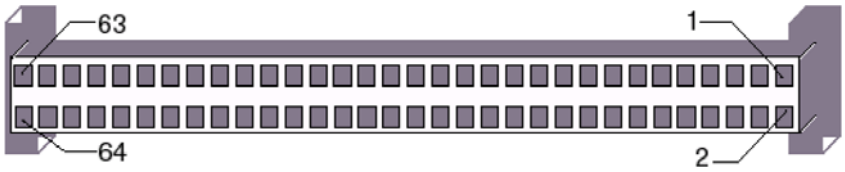


Table E-6 PMC Connector Pinout (J12, J22, J32)

PMC Connector (J12, J22, J32)				PMC Connector (J12, J22, J32)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	+12V	2	TRST#*	33	GND	34	N/C
3	TMS*	4	TDO*	35	TRDY#	36	+3.3V
5	TDI*	6	GND	37	GND	38	STOP#
7	GND	8	N/C	39	PERR#	40	GND
9	N/C	10	N/C	41	+3.3V	42	SERR#
11	PUP	12	+3.3V	43	CBE[1]#	44	GND
13	RST#	14	PDN1#	45	AD[14]	46	AD[13]
15	+3.3V	16	PDN2#	47	M66EN	48	AD[10]
17	PME#	18	GND	49	AD[8]	50	+3.3V
19	AD[30]	20	AD[29]	51	AD[7]	52	REQB#
21	GND	22	AD[26]	53	+3.3V	54	GNTB#
23	AD[24]	24	+3.3V	55	N/C	56	GND
25	IDSEL	26	AD[23]	57	N/C	58	N/C
27	+3.3V	28	AD[20]	59	GND	60	N/C
29	AD[18]	30	GND	61	ACK64#	62	+3.3V
31	AD[16]	32	CBE[2]#	63	GND	64	N/C

*These signals are specific to JTAG and reserved for factory use only.

E.7.3 PMC Connectors and Pinouts (J13, J23, J33)

Figure E-7 Connector (J13, J23, J33)

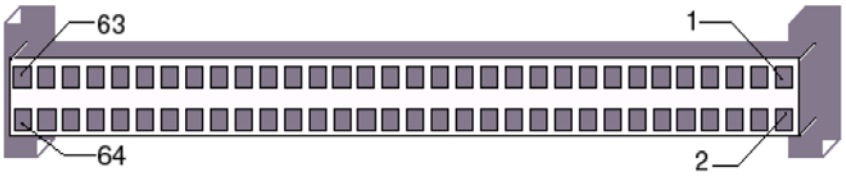


Table E-7 PMC Connector and Pinout (J13, J23, J33)

PMC Connector (J13, J23, J33)				PMC Connector (J13, J23, J33)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	N/C	2	GND	33	GND	34	AD[48]
3	GND	4	CBE[7]#	35	AD[47]	36	AD[46]
5	CBE[6]#	6	CBE[5]#	37	AD[45]	38	GND
7	CBE[4]#	8	GND	39	VCC_PMC_IO	40	AD[44]
9	VCC_PMC_IO	10	PAR64	41	AD[43]	42	AD[42]
11	AD[63]	12	AD[62]	43	AD[41]	44	GND
13	AD[61]	14	GND	45	GND	46	AD[40]
15	GND	16	AD[60]	47	AD[39]	48	AD[38]
17	AD[59]	18	AD[58]	49	AD[37]	50	GND
19	AD[57]	20	GND	51	GND	52	AD[36]
21	VCC_PMC_IO	22	AD[56]	53	AD[35]	54	AD[34]
23	AD[55]	24	AD[54]	55	AD[33]	56	GND
25	AD[53]	26	GND	57	VCC_PMC_IO	58	AD[32]
27	GND	28	AD[52]	59	N/C	60	N/C
29	AD[51]	30	AD[50]	61	N/C	62	GND
31	AD[49]	32	GND	63	GND	64	N/C

E.7.4 PMC Connector and Pinout (J14)

J14 supplies the PCI Express interface signals for PMC site 0, through the VME backplane connector P2.

Figure E-8 Connector (J14)

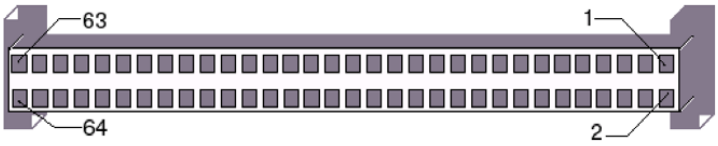


Table E-8 PMC Connector and Pinout (J14)

Signal	Pin	Pin	Signal
PMC0_IO_D1	1	2	PMC0_IO_Z1
PMC0_IO_D2	3	4	PMC0_IO_D3
PMC0_IO_Z3	5	6	PMC0_IO_D4
PMC0_IO_D5	7	8	PMC0_IO_Z5
PMC0_IO_D6	9	10	PMC0_IO_D7
PMC0_IO_Z7	11	12	PMC0_IO_D8
PMC0_IO_D9	13	14	PMC0_IO_Z9
PMC0_IO_D10	15	16	PMC0_IO_D11
PMC0_IO_Z11	17	18	PMC0_IO_D12
PMC0_IO_D13	19	20	PMC0_IO_Z13
PMC0_IO_D14	21	22	PMC0_IO_D15
PMC0_IO_Z15	23	24	PMC0_IO_D16
PMC0_IO_D17	25	26	PMC0_IO_Z17
PMC0_IO_D18	27	28	PMC0_IO_D19
PMC0_IO_Z19	29	30	PMC0_IO_D20
PMC0_IO_D21	31	32	PMC0_IO_Z21
PMC0_IO_D22	33	34	PMC0_IO_D23
PMC0_IO_Z23	35	36	PMC0_IO_D24
PMC0_IO_D25	37	38	PMC0_IO_Z25
PMC0_IO_D26	39	40	PMC0_IO_D27
PMC0_IO_Z27	41	42	PMC0_IO_D28
PMC0_IO_D29	43	44	PMC0_IO_Z29
PMC0_IO_D30	45	46	PMC0_IO_Z31
PMC0_IO_A1	47	48	PMC0_IO_A2
PMC0_IO_A3	49	50	PMC0_IO_A4
PMC0_IO_A5	51	52	PMC0_IO_A6
PMC0_IO_A23	53	54	PMC0_IO_A24
PMC0_IO_A25	55	56	PMC0_IO_A26
PMC0_IO_A27	57	58	PMC0_IO_A28
PMC0_IO_A29	59	60	PMC0_IO_A30
PMC0_IO_A31	61	62	PMC0_IO_A32
PMC0_IO_C18	63	64	PMC0_IO_C19

E.8 EXP238 XMC Connectors and Pinouts (J15, J25, J35)

Figure E-9 XMC Connector (J15, J25, J35)

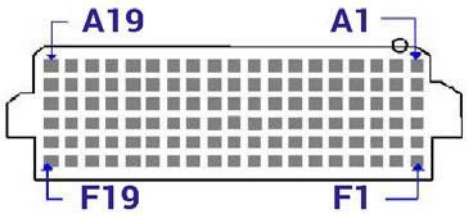


Table E-9 XMC Connector and Pinout (J15-Site 0; J25-Site 1; J35-Site 2)

Row A		Row B		Row C		Row D		Row E		Row F	
1	TX0+	1	TX0-	1	3.3V	1	TX1+	1	TX1-	1	5V
2	GND	2	GND	2	TRST#*	2	GND	2	GND	2	RST_OUT#
3	TX2+	3	TX2-	3	3.3V	3	TX3+	3	TX3-	3	5V
4	GND	4	GND	4	TCK*	4	GND	4	GND	4	RST_IN#
5	N/C	5	N/C	5	3.3V	5	N/C	5	N/C	5	5V
6	GND	6	GND	6	TMS*	6	GND	6	GND	6	12V
7	N/C	7	N/C	7	3.3V	7	N/C	7	N/C	7	5V
8	GND	8	GND	8	TDI*	8	GND	8	GND	8	-12V
9	N/C	9	N/C	9	N/C	9	N/C	9	N/C	9	5V
10	GND	10	GND	10	TDO*	10	GND	10	GND	10	GA0/GND
11	RX0+	11	RX0-	11	MBIST#	11	RX1+	11	RX1-	11	5V
12	GND	12	GND	12	GA1	12	GND	12	GND	12	XMC_PRS#
13	RX2+	13	RX2-	13	3.3V	13	RX3+	13	RX3-	13	5V
14	GND	14	GND	14	GA2	14	GND	14	GND	14	MSDA
15	N/C	15	N/C	15	N/C	15	N/C	15	N/C	15	5V
16	GND	16	GND	16	NVMRO	16	GND	16	GND	16	MSCL
17	N/C	17	N/C	17	N/C	17	N/C	17	N/C	17	N/C
18	GND	18	GND	18	N/C	18	GND	18	GND	18	N/C
19	CLK+	19	CLK-	19	N/C	19	N/C	19	N/C	19	N/C

* These signals are specific to JTAG and reserved for factory use only.

E.9 EXP238 Backplane Connectors

E.9.1 EXP238 VMEbus Connector (P1)

Figure E-10 VME Connectors (P1, P2)

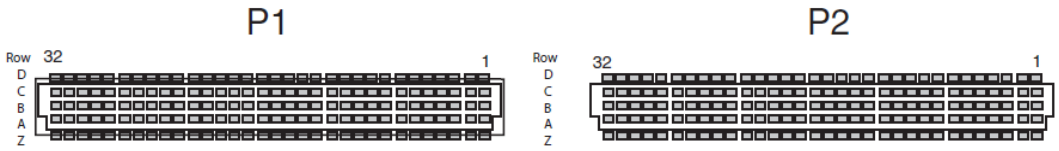


Table E-10 EXP238 VME Connector (P1)

Pin	Row Z	Row A	Row B	Row C	Row D
1	TRST#*	N/C	N/C	N/C	+5V
2	GND	N/C	N/C	N/C	GND
3	TCK*	N/C	N/C	N/C	N/C
4	GND	N/C	BG0IN_OUT#	N/C	N/C
5	TDO*	N/C	BG0IN_OUT#	N/C	N/C
6	GND	N/C	BG1IN_OUT#	N/C	N/C
7	TDI*	N/C	BG1IN_OUT#	N/C	N/C
8	GND	N/C	BG2IN_OUT#	N/C	N/C
9	TMS*	GND	BG2IN_OUT#	GND	N/C
10	GND	N/C	BG3IN_OUT#	N/C	N/C
11	N/C	GND	BG3IN_OUT#	N/C	N/C
12	GND	N/C	N/C	N/C	N/C
13	N/C	N/C	N/C	N/C	N/C
14	GND	N/C	N/C	N/C	N/C
15	N/C	GND	N/C	N/C	N/C
16	GND	N/C	N/C	N/C	N/C
17	N/C	GND	N/C	N/C	N/C
18	GND	N/C	N/C	N/C	N/C
19	N/C	GND	N/C	N/C	N/C
20	GND	N/C	GND	N/C	N/C
21	N/C	IACKIN_OUT#	N/C	N/C	N/C
22	GND	IACKIN_OUT#	N/C	N/C	N/C
23	N/C	N/C	GND	N/C	N/C
24	GND	N/C	N/C	N/C	N/C
25	N/C	N/C	N/C	N/C	N/C
26	GND	N/C	N/C	N/C	N/C
27	N/C	N/C	N/C	N/C	N/C
28	GND	N/C	N/C	N/C	N/C
29	N/C	N/C	N/C	N/C	N/C
30	GND	N/C	N/C	N/C	N/C
31	N/C	-12V	N/C	+12V	GND
32	GND	+5V	+5V	+5V	+5V

* These signals are specific to JTAG and reserved for factory use only.

E.9.2 EXP238 VMEbus Connector (P2)

The following table lists the pin assignments of connector P2. Row B of the connector is compatible to connector P2 of the VMEbus specifications ANSI/VITA 1 (VME64) and ANSI/VITA 1.1 (VME64x).

Rows A and C are not connected.

Table E-11 VME Connector Pinouts (P2)

Pin	Row Z	Row A	Row B	Row C	Row D
1	PMC0_IO_Z1	N/C	+5V	N/C	PMC0_IO_D1
2	GND	N/C	GND	N/C	PMC0_IO_D2
3	PMC0_IO_Z3	N/C	N/C	N/C	PMC0_IO_D3
4	GND	N/C	N/C	N/C	PMC0_IO_D4
5	PMC0_IO_Z5	N/C	N/C	N/C	PMC0_IO_D5
6	GND	N/C	N/C	N/C	PMC0_IO_D6
7	PMC0_IO_Z7	N/C	N/C	N/C	PMC0_IO_D7
8	GND	N/C	N/C	N/C	PMC0_IO_D8
9	PMC0_IO_Z9	N/C	N/C	N/C	PMC0_IO_D9
10	GND	N/C	N/C	N/C	PMC0_IO_D10
11	PMC0_IO_Z11	N/C	N/C	N/C	PMC0_IO_D11
12	GND	N/C	GND	N/C	PMC0_IO_D12
13	PMC0_IO_Z13	N/C	+5V	N/C	PMC0_IO_D13
14	GND	N/C	N/C	N/C	PMC0_IO_D14
15	PMC0_IO_Z15	N/C	N/C	N/C	PMC0_IO_D15
16	GND	N/C	N/C	N/C	PMC0_IO_D16
17	PMC0_IO_Z17	N/C	N/C	N/C	PMC0_IO_D17
18	GND	N/C	N/C	N/C	PMC0_IO_D18
19	PMC0_IO_Z19	N/C	N/C	N/C	PMC0_IO_D19
20	GND	N/C	N/C	N/C	PMC0_IO_D20
21	PMC0_IO_Z21	N/C	N/C	N/C	PMC0_IO_D21
22	GND	N/C	GND	N/C	PMC0_IO_D22
23	PMC0_IO_Z23	N/C	N/C	N/C	PMC0_IO_D23
24	GND	N/C	N/C	N/C	PMC0_IO_D24
25	PMC0_IO_Z25	N/C	N/C	N/C	PMC0_IO_D25
26	GND	N/C	N/C	N/C	PMC0_IO_D26
27	PMC0_IO_Z27	N/C	N/C	N/C	PMC0_IO_D27
28	GND	N/C	N/C	N/C	PMC0_IO_D28
29	PMC0_IO_Z29	N/C	N/C	N/C	PMC0_IO_D29
30	GND	N/C	N/C	N/C	PMC0_IO_D30
31	PMC0_IO_Z31	N/C	GND	N/C	GND
32	GND	N/C	+5V	N/C	+5V

F • Processor Speed and Temperature

The processor speed and the temperature are inter-dependent. This means that for a given temperature, a maximum processor speed is achievable before throttling, and conversely for a given processor speed before throttling, a maximum temperature is achievable. This is further affected by the build level, which dictates the maximum ambient temperature at which the board can operate, refer to Section A.8, "Environmental Compliance".

NOTE

The processor speed can be set from the UEFI via the **Chipset -CPU Speed Locking Configuration** menu. See Section C.6.1, "CPU Speed Locking Configuration".

The thermal data from the tables below was taken while the units were running multi-threaded test software used to stress the CPU, memory and I/O functions simultaneously. This test load is generally heavier than a standard embedded application. There may be some variance in the user's thermal results based on the end application. Please contact Abaco Systems Sales or Technical Support for any further thermal details or discussions relating to your specific application.

F.1 Quad Core (Xeon) 45W, 3.0 GHz Processor

Table F-1 Maximum Operating Frequency versus Max Temperature for Quad Processor

		Maximum Operating		5V DC A			
CPU Power	Build Level	Frequency	Temperature	Min	Avg	Max	Dissipation Method
45W	1	3.0 GHz	55°C	7.8	9.6	10.8	300 LFM
	2	3.0 GHz	60°C	7.9	9.8	10.8	
		2.7 GHz	65°C	7.5	8.7	9.6	

F.2 Quad Core (Xeon) 25W, 2.2 GHz LP Processor

Table F-2 Maximum Operating Frequency versus Max Temperature for Quad LP Processor

		Maximum Operating		5V DC A			
CPU Power	Build Level	Frequency	Temperature	Min	Avg	Max	Dissipation Method
25W	1	2.2 GHz	55°C	5.8	6.3	7.0	300 LFM
	2	2.2 GHz	65°C	5.9	6.5	7.2	

G • Statement of Volatility

G.1 Volatile Memory

This product contains volatile memory, i.e. memory in which the contents are lost when power is removed.

Table G-1 Volatile Memory

Type of Memory	Size	User Modifiable	User Data Access	Function	Process to Clear
SDRAM – 1.2V	8, 16	Yes	Yes	Contains run-time data	powerdown

G.2 Non-Volatile Memory

This product contains non-volatile memory, i.e., memory in which the contents are retained when power is removed.

Table G-2 Non-Volatile Memory

Type of Memory	Size	User Modifiable	User Data Access	Function	Process to Clear
U549, U508 NVRAM SPI 3.3V SPI Flash Non-Volatile RAM	512 KBytes	Yes	Yes	Storage of user/BIT information	This memory space can be cleared by any utility capable of writing IO and memory space
U180, U181, U182 SPI Flash 3.3V	16 MBytes	Yes	Yes	Contains UEFI code, ME Firmware and UEFI settings	This memory space can be cleared by any utility capable of writing to the PCH SPI bus
P7 (Optional) SATA M.2 NAND Drive, 3.3V	32/128 GBytes	Yes	Yes	Solid State Flash Drive	Any hard drive formatting utility
U150 FPGA 3.3V, 2.5V, 1.2V glue	N/A	No	No	Powerup/reset logic, LPC registers, Timers, Watchdog, NVRAM Access	JTAG via rear connector
U437, U438 I^2C EEPROM 3.3V	4 Kbits	Yes	Yes	SPD information for DDR4 Memory	This memory space can be cleared by any utility capable of writing to the PCH I^2C bus
U575 SPI Flash 3.3V	256 Mbit	No	No	VME FPGA	Test Card via Test Connector
U111, U121, U131 SPI Flash 3.3V	2 KBytes	Yes	Yes	Storage of Ethernet Configuration	This memory space can be cleared by any utility capable of writing to the LAN SPI bus

NOTE

In normal operation all non-volatile memory, except the NVRAM (U508, U549) and optional SATA SSD M.2 (P7), remain write protected. The M.2 *cannot* be write protected. The NVRAM device may be write protected or write enabled by adjusting the NVRAM Write Protection setting in the UEFI setup. See Section C.6.2 for details on how to control the write protection of the NVRAM.

Abaco Systems Information Centers

Americas:
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Europe, Middle East and Africa:
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Publication No. 500-9300007880-000 Rev. M