ABOS-9XXC Series

15.6”, 21.5” Button-Integrated Panel PC

User Manual

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Revision History

Reversion	Date	Description
1.0	2024/01/19	Official Version
1.1	2024/6/15	
1.2	2024/8/10	
1.3	2024/9/24	

Warning!_____

This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, it may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

Electric Shock Hazard

– Do not operate the machine with its back cover removed. There are dangerous high voltages inside.

– Provide protective earthing for handling the device.

Disclaimer

This information in this document is subject to change without notice. In no event shall Aplex Technology Inc. be liable for damages of any kind, whether incidental or consequential, arising from either the use or misuse of information in this document or in any related materials.

Pressure Testing Screw Warning:

Before deploying your ABOS series system, it is crucial to ensure that the pressure testing screw is securely tightened. This precaution is essential to prevent potential issues arising from rapid air pressure changes during transportation, particularly in air shipments with unpressurized cabins.

Note: The pressure testing screw is intentionally loosened by half a turn before shipment.

Instructions for Tightening the Pressure Testing Screw:

Prepare Tools:
Obtain a 3mm hex screwdriver.
Locate the Screw:

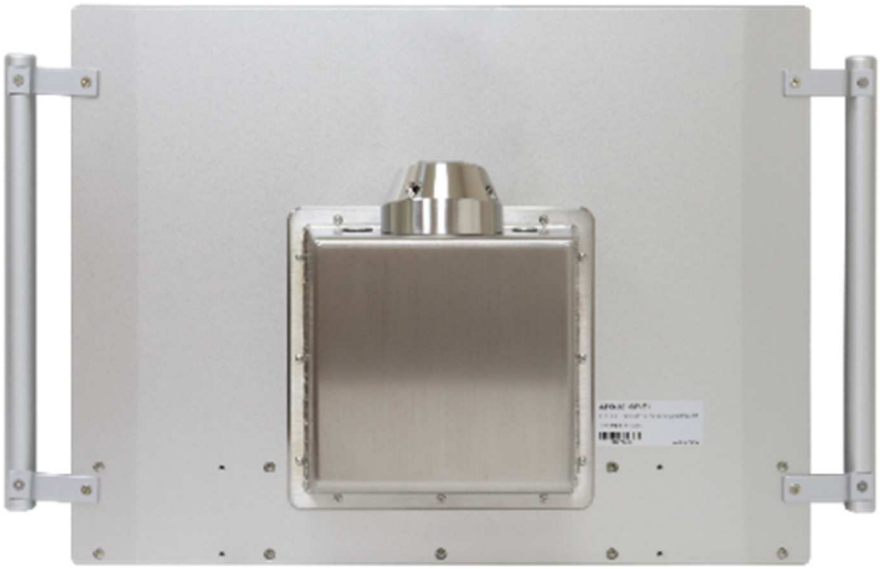
Identify the pressure testing screw, indicated within a circle on your system.
Tighten Clockwise:

Using the 3mm hex screwdriver, tighten the pressure testing screw clockwise until it is securely in place.
Recommended Torque:

Apply a torque of 8~10 kgf-cm for optimal functionality.
Caution:

Failure to tighten the pressure testing screw may lead to performance issues or damage during operation.
Note to Users:

Always check and tighten the pressure testing screw upon receiving the system, ensuring its stability before deployment. Neglecting this step may compromise the functionality of your ABOS series system.
For any questions or concerns regarding this procedure, please contact APLEX Technology's customer support.



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Chapter 1 Getting Started

1.1 Features

- 15.6”/21.5” FHD TFT LCD Panel PC
- Intel® 11th Gen. (Tiger Lake-UP3) Processors
- 16:9 Widescreen with P-CAP Multi-touch Control
- Built-in Functional Buttons for Intuitive Operation
- Gap-free sealing and Slim Front Frame architecture at front bezel
- Top/Bottom Swing Arm Mounting
- IP65 Full-sealed with Anti-Corrosion Enclosure (with Swig ARM Kit)
- Available with Configurable Button Area for the installation of Hard-wired Elements
- DC 9~36V wide range power input

1.2 Specifications

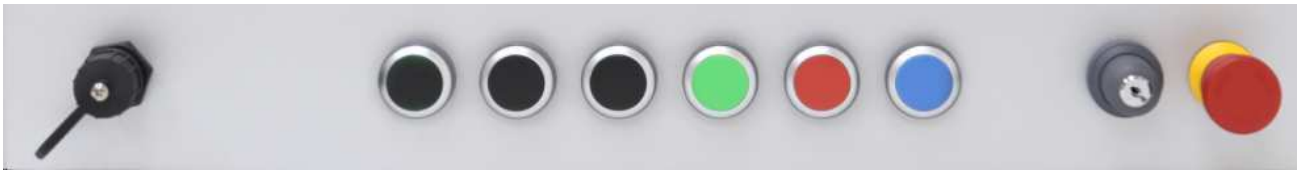
	ABOS-916CP	ABOS-921CP
System		
CPU	Onboard Intel® 11th Gen (Tiger Lake-UP3) Processors: Core i3-1115G4E (2C, 2.2 GHz, 15W TDP) Core i5-1145G7E (4C, 1.5 GHz, 15W TDP)	
Memory	2 x SO-DIMM up to 64GB DDR4 3200MHz (Dual Channel, Non-ECC)	
LVDS	1 x 18/24 bit Dual Channel	
Outside IO Port		
USB	1 x USB2.0 (Type A)-Front 4 x USB 3.2(Type-A)-Rear 1 x USB 3.2 GEN2 Type C-Rear	
Serial/Parallel	1 x COM (RS-232/422/485, default)-COM1 1 x COM(RS-232/422/485, support 5V/12V/RI, option)-COM2	
LAN	1 x Intel i219LM RJ45 GbE LAN 1 x Intel i225LM, RJ45 2.5G LAN	
Power	1 x 3-pin Phoenix Connector for DC power	
Storage Space		
Storage	1 x M.2 M-Key 2280 (PCIex4) Socket for Optional PCIe/NVME SSD	
Expansion		

Expansion Slot	1 x M.2 2230 E-Key (PCIex2+USB2.0) socket for WIFI/BT and Antenna at rear side (option) 1 x Full-size mPCIe/mSATA (mSATA as default, select by BIOS) 1 x Nano SIM Card

Functional Buttons: Supports RAFI RAFIX-22-FS Series

For the push button extensions can be used to control the central functions of a machine or system such as emergency stop, start or stop by means of electromechanical keys and are already mounted ex factory.

Then specific ordering options are available.



Default Button:	Option Button:
1 x USD2.0 Type A with Cover 1 x Push Button/Green for START 1 x Push Button/Red for STOP 1 x Push Button/Blue for Reset 1 x Emergency Stop Button	3 x Push Button/Black for Self-Defined 1 x Key switch

Display – Standard LCD

Display Type	15.6” TFT LCD	21.5” TFT LCD
Max. Resolution	1920 x 1080	1920 x 1080
Max. Color	16.7M	16.7M
Luminance (cd/m^2)	500 nits	250 nits
Contrast Ratio	1000:1	1000:1
Viewing Angle(H/V)	178/178	178/178
Backlight Lifetime	50,000hrs	50,000hrs
Option	Optical bonding	

Display – High Brightness LCD (option)

Display Type	15.6” TFT LCD	21.5” TFT LCD
Max. Resolution	1920 x 1080	1920 x 1080
Max. Color	16.7M	16.7M
Luminance (cd/m^2)	1000 nits	1000 nits
Contrast Ratio	1000:1	1000:1

Viewing Angle(H/V)	170/170	174/174
Backlight Lifetime	50,000hrs	30,000hrs
Option	Optical bonding	
Touch Screen		
Type	Projected capacitive touch screen	
Interface	USB	
Light Transmission	Projected capacitive touch screen: over 90%	
Power		
Power Input	DC 9~36V onboard	
Power Consumption	MAX:34.99W	MAX:34.05W
Mechanical		
Construction	Aluminum CNC enclosure Rear Housing: Stainless Steel 304	
Mounting	SWING ARM (support CP-40 Rittal)	
IP Rating	Total IP65 (with Swing ARM kit)	
Bracket (Option)	Left-Right Handle: Aluminum CNC Keyboard Holder: Aluminum CNC	
Dimension (mm)	409.9 x 341.1 x 162 (Without Handle and Holder)	545.8 x 418 x 162 (Without Handle and Holder)
Net Weight(Kg)	10.23	17.5
Environmental		
Operating temperature	0~50°C	
Storage temperature	-30~70°C	
Storage humidity	10 to 90% @ 40°C, non- condensing	
Certification	Meet CE / FCC Class A	
Operating System Support	Windows 10 IoT ENT LTSC/ Windows 11 IoT/Linux Kernel 5.15(Ubuntu 20.04/22.04)	

1.3 Dimensions

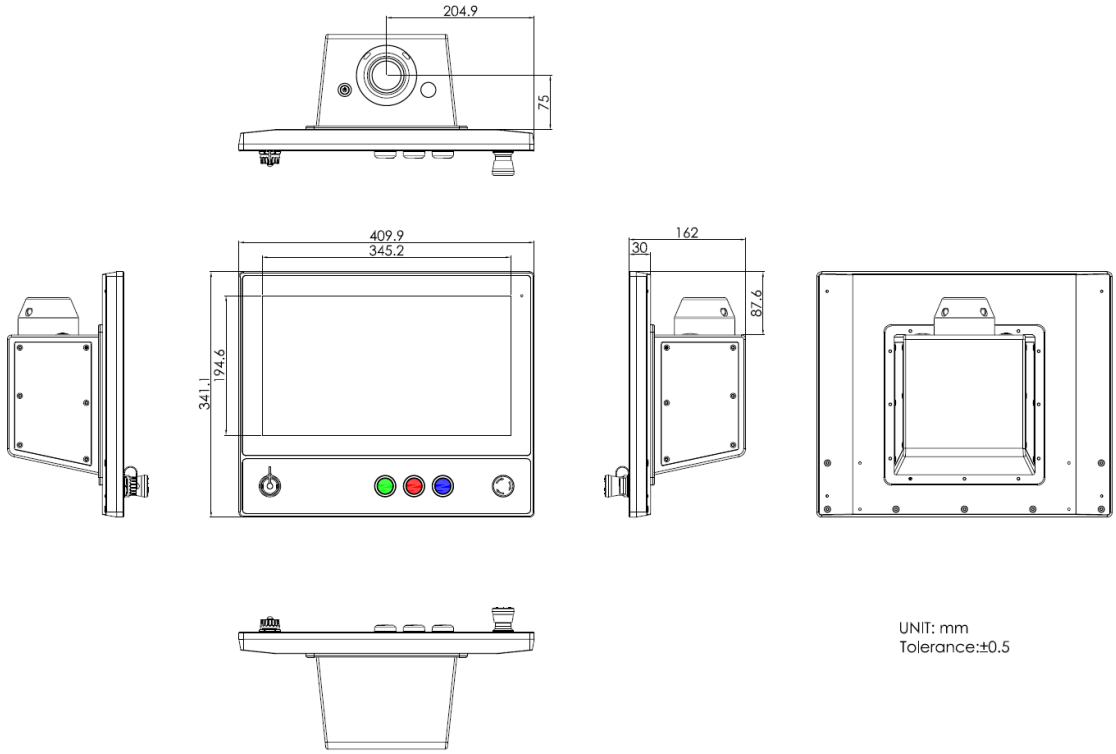


Figure 1.1: Dimensions of ABOS-916CP(H)

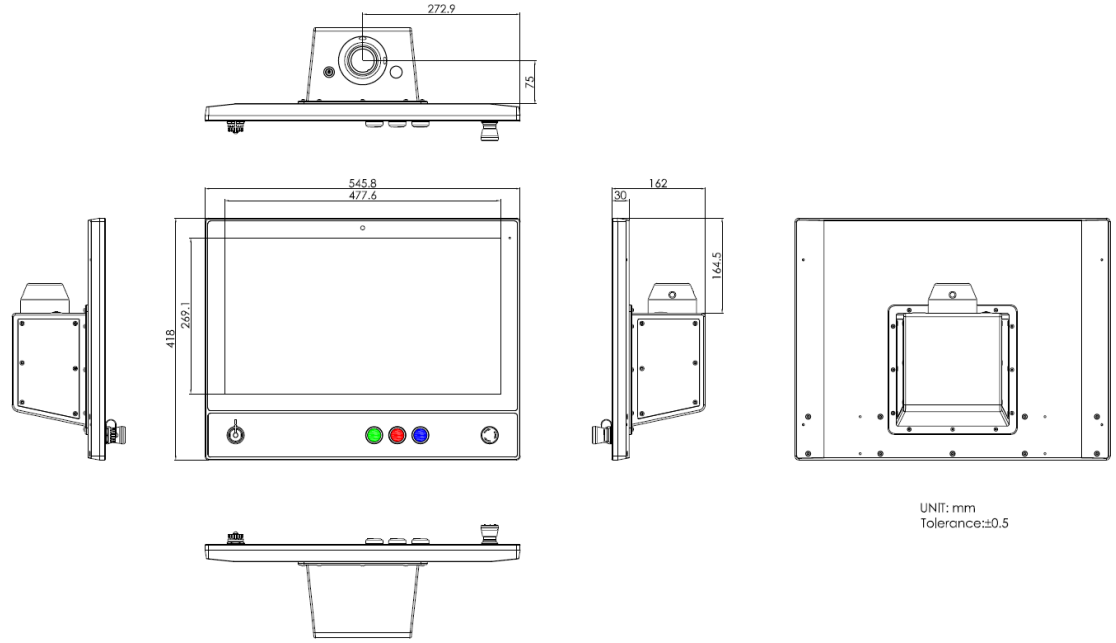


Figure 1.2: Dimensions of ABOS-921CP(H)

1.4 Brief Description of ABOS-9XXC Series

The ABOS-9XXC series is a state-of-the-art stainless steel panel PC featuring Intel 11th Gen (Tiger Lake-UP3) technology. With an IP65 rating, Swing ARM kits, and 15.6”/21.5” TFT LCD displays, it excels in versatility. Robust Aluminum CNC and Stainless Steel 304 construction, wide DC power input, and options for high brightness LCD and optical bonding make it adaptable for diverse environments. The series supports responsive capacitive touch, and its configurable button area enhances customization for specialized applications. Ideal for industrial and commercial setups, it seamlessly integrates cutting-edge performance with rugged design.

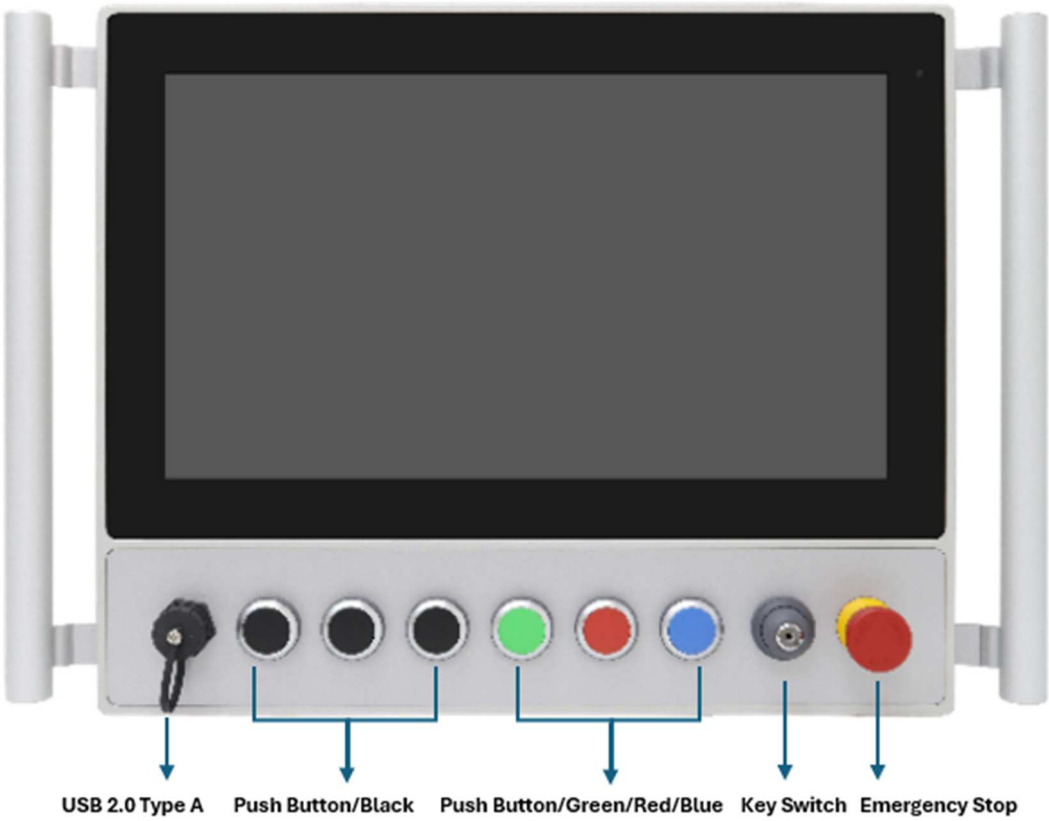


Figure 1.3: Front View ABOS-916CP

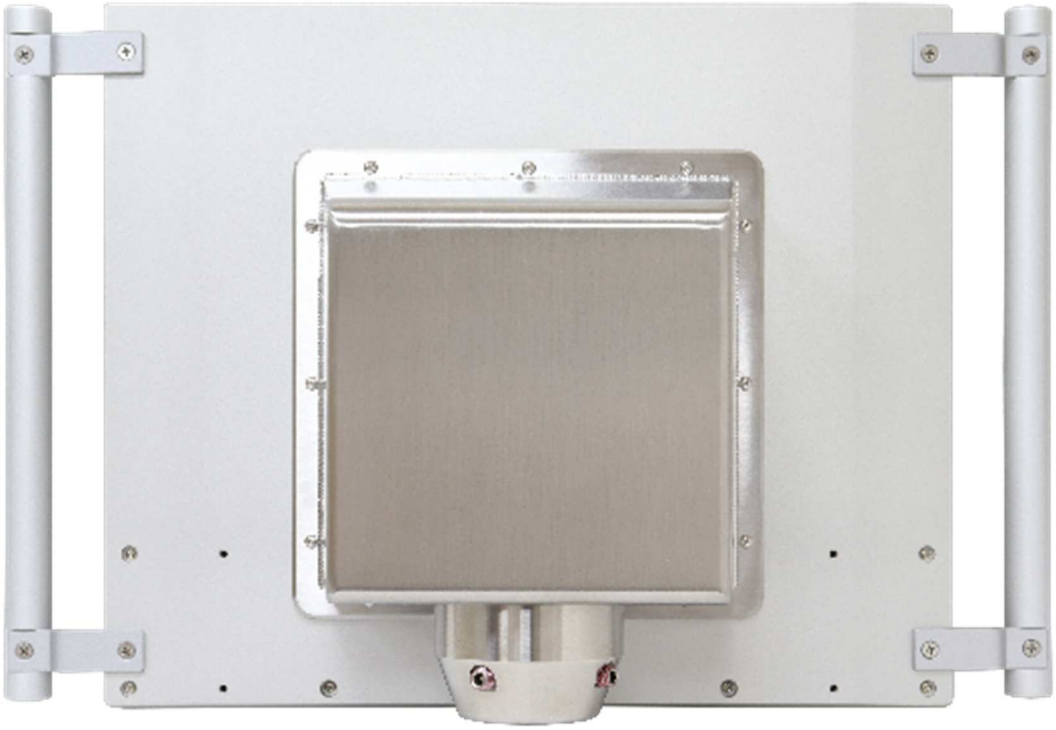


Figure 1.4: Rear View of ABOS-916CP

Figure 1.5: Front View ABOS-921CP

Figure 1.6: Rear View of ABOS-921CP

Chapter 2 Hardware

2.1 Motherboard Introduction

Standard 3.5" subcompact board developed on the basis of Intel 11th Generation Core™/Celeron Processor, which provides abundant peripheral interfaces to meet the needs of different customers. Also, it features one mPCIe/mSATA, dual GbE ports, 2-COM and 4 x USB3.2 Gen 2 Ports; one HDMI, one VGA and one LVDS interface.

2.2 Specifications & Dimensions

Specifications	
Board Size	146mm x 107.7mm
CPU Support	Intel® Core™ i3-1115G4E(2C/4T, 2.20GHz, up to 3.90GHz, TDP 15W) Intel® Core™ i5-1145G7E(4C/8T, 1.50GHz, up to 4.10GHz, TDP 15W)
Chipset	SOC
Memory Support	DDR4 up to 3200MHz, Dual Channel SODIMM x2, up to 64GB, IBECC
Graphics	Intel® UHD Graphics Intel® Iris® Xe Graphics
Display Mode	1 x HDMI 2.0b 2 x DP 1.4a
Multi Display	3 Simultaneous Displays
Wake on LAN	Yes
BIOS	AMI UEFI
SATA	1 x SATAIII (6.0Gbps) 1 x +5V SATA Power Connector
Video	LVDS/ eDP x 1 (default: LVDS) eDP: up to 1080P@60Hz
USB	2 x USB 2.0
Serial	3 x RS232/RS422/RS485 port, (COM1, COM3, COM4) 1 x RS232/RS422/RS485 port, support 5V/12V/RI(COM2)
Digital I/O	8-bit digital I/O 4-bit digital Input

	4-bit digital Output
Battery	Lithium Battery 3V/240mAh
SMBus/I2C	I2C/SMBus x 1 (Default: SMBus)
SIM	Nano-SIM x 1
Audio	Support Audio via Realtek ALC897/892 audio codec Audio Interface: Line-in/Line-out/MIC 1x Audio Header
Expansion Bus	1 x Full-size mPCIe/mSATA slot (mSATA as default, , select by BIOS) M.2 M-Key 2280 x 1 (PCIe [x4]) M.2 E-Key 2230 x 1 (PCIe, USB2.0)
FAN	Smart Fan x 1
Touch Ctrl	4/5/8-wire touch controller(option)
Power Management	Wide Range DC+9V~36V (+12V option) 1 x 2-pin Phoenix connector Power supply type: AT/ATX
Switches and LED Indicators	1 x Power on/off switch 1 x Buzzer
External I/O port	4 x USB 3.2 Gen 2 Ports 1 x USB 3.2 Gen 2 Type C (PD5V/3A) 2 x RJ45 GbE LAN Ports 1 x HDMI 2.0b 2 x DP 1.4a 1 x DP 1.4 (Type C)
Temperature	Operating: 0℃ to 60℃ Storage: -40℃ to 80℃
Humidity	0% - 90% relatively, non-condensing, operating
Power Consumption	Typical: 4.96A at +12V, Intel® i7-1185G7E, DDR4 3200MHz 32GB x 2 Maximum: 7.32A at +12V, Intel® i7-1185G7E, DDR4 3200MHz 32GB x 2
Watchdog Timer	255 Level
MTBF (Hrs)	329,884
EMI/EMS	CE/FCC class A

2.3 Jumpers and Connectors Location

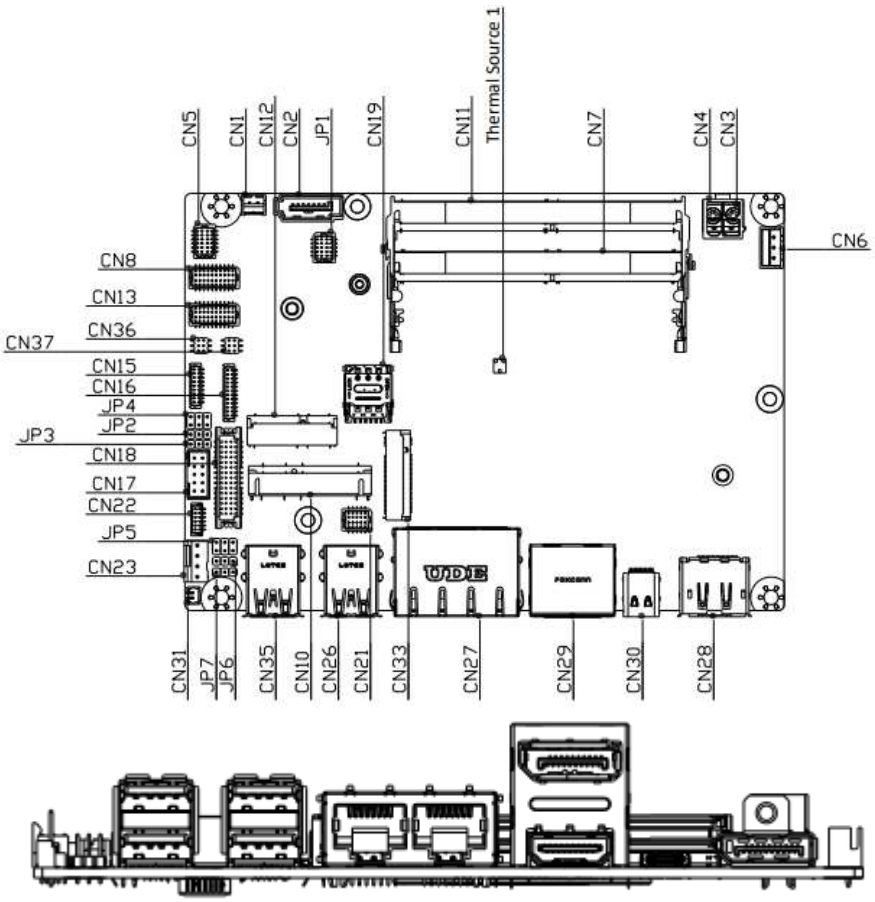


Figure 2.2: Jumpers and Connectors Location- Board Top

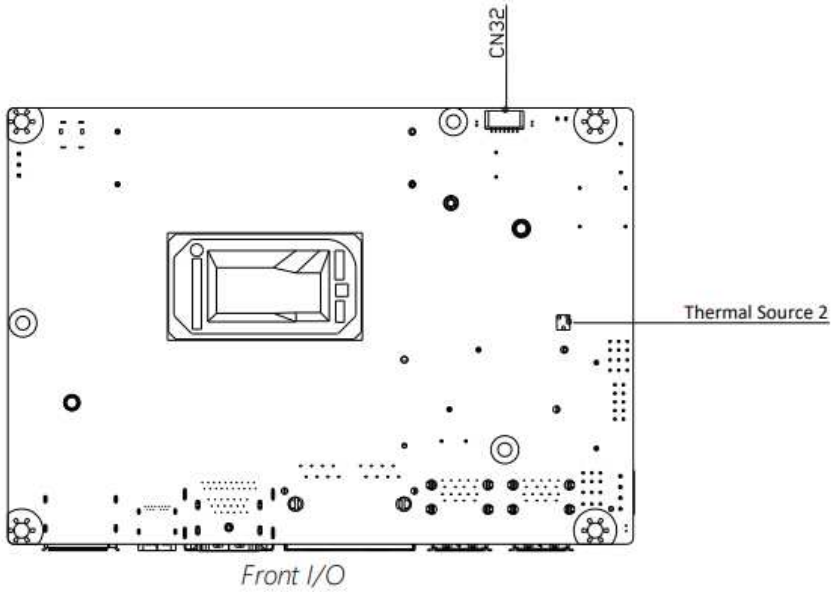


Figure 2.3: Jumpers and Connectors Location- Board Bottom

Chapter 3 BIOS Setup

3.1 System Test and Initialization

The board uses certain routines to perform testing and initialization during the boot up sequence . Ifan error, fatal or non-fatal, is encountered, the module will output a few short beeps or display an error message. The module can usually continue the boot up sequence with non-fatal errors.
The system configuration verification routines check the current system configuration against the values stored in the CMOS memory and BIOS NVRAM. If a system configuration is not found or an erroris detected, the module will load the default configuration and reboot automatically.

There are four situations in which you will eed to setup system configuration:
1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration was restt by the Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.
The system CMOS memory has an integral lithium battery backup for data retention.
You will need to replace the battery unit when it runs down.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurati ons., which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter B1OS Setup, press <Del> or <ESC> immediately while your computer is powering up.
The function for each interface can be found below.

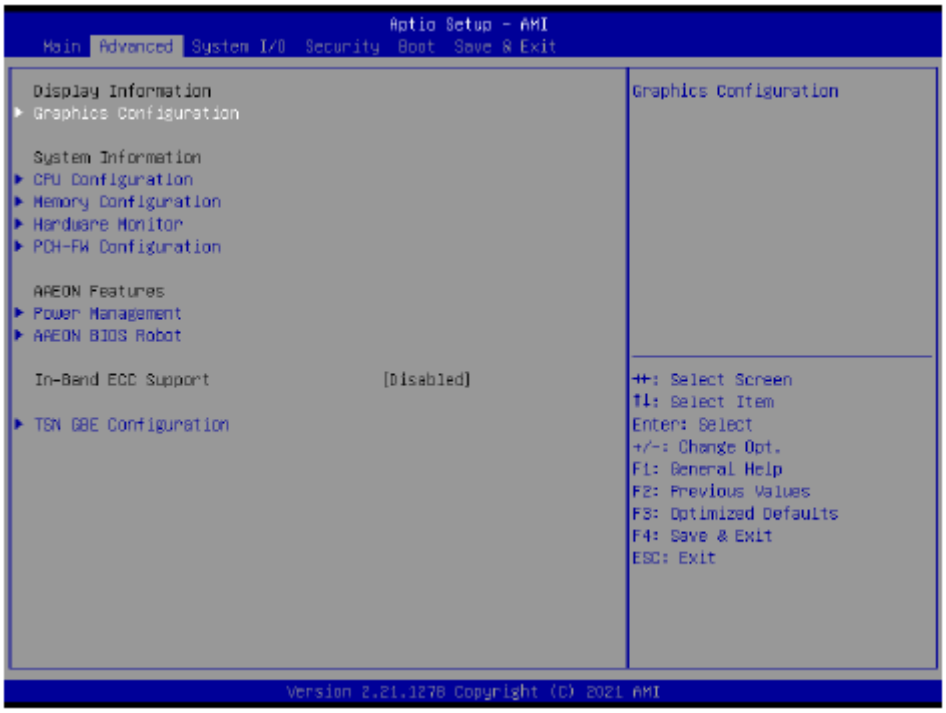
Main - Date and time can be set here. Press <Tab> to switch between date elements
Advanced -Access advanced hardware settings and Hardware Monitor
Chipset- Chipset settings and options
Security -Set admin and user passwords, access secure boot options

Boot-Boot options including 8BS priority and Quiet Boot options

Save & Exit --Save your changes and ext the program

3.3 Setup Submenu:Main

3.4 Setup Submenu: Advanced

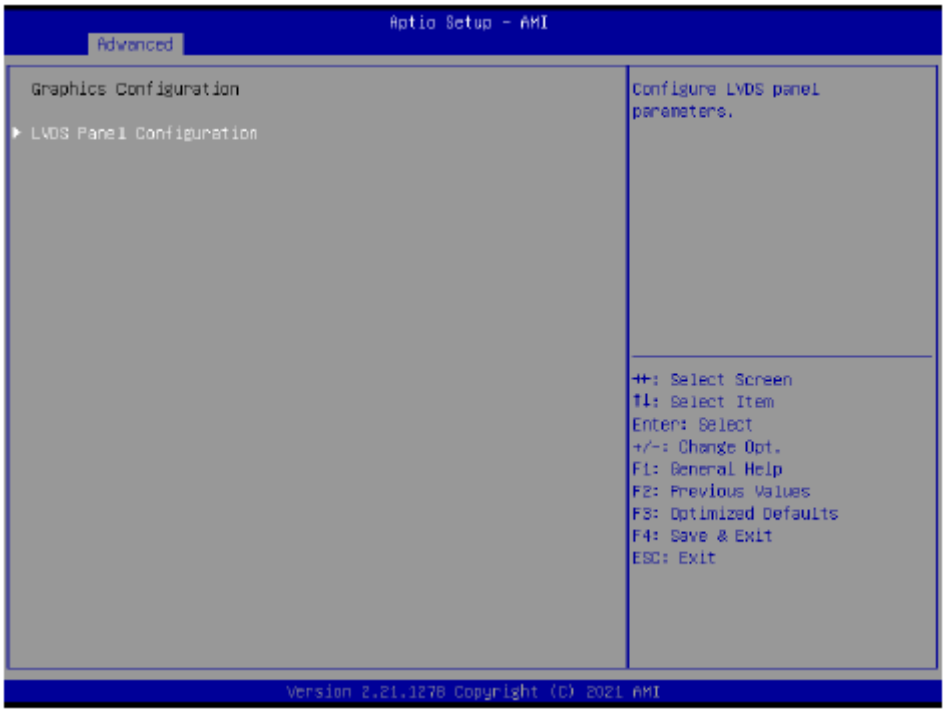


Options Summary		
In-Band ECC Support	Disabled	
	Enabled	Optimal Default; Failsafe Default
Enable/Disabled In-Band ECC Support		
In-Band ECC Error Injection	Enabled	
	Disabled	Optimal Default, Failsafe Default
By enabling this Error Injection feature, the user acknowledges the security risks. Enabling Error Injection allows attackers who have access to the Host Operating System to inject IBECC errors that can cause unintended memory corruption and enable the leak of security data in the BIOS stolen memory regions.		
In-Band ECC Operation Mode	0	
	1	
	2	Optimal Default, Failsafe Default
0: Functional Mode protects requests based on the address range, 1: Makes all requests non-protected and ignore range checks, 2: Makes all requests protected and ignore range checks		

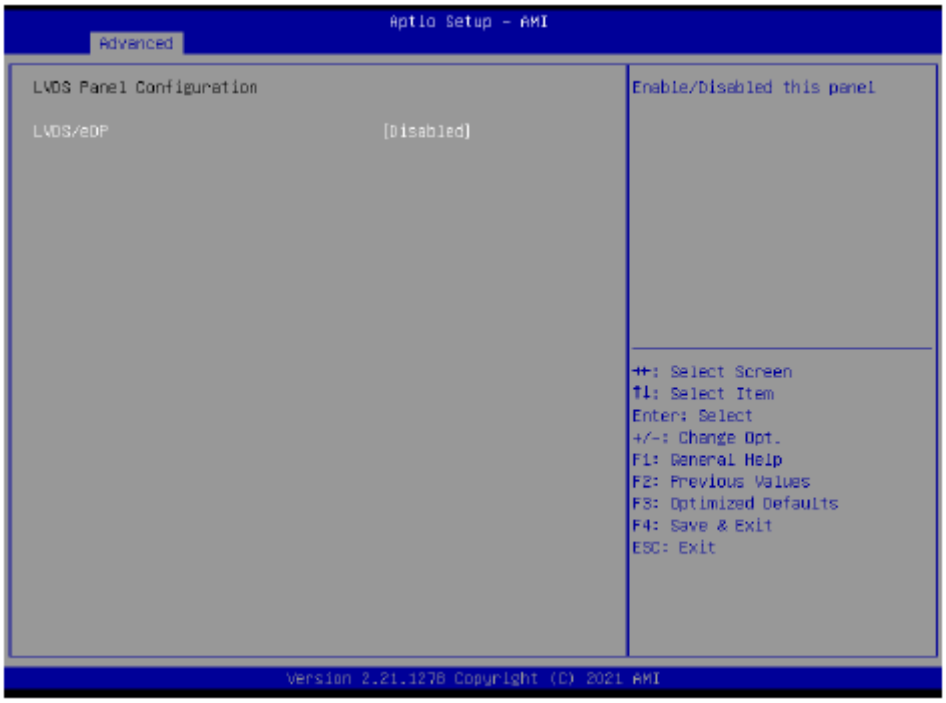
Options Summary		
IBECC Protect Region 0-7	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disabled In-Band ECC for Region 0-7		

Note: In-Band ECC Support availability depends on CPU.

3.4.1 Graphics Configuration



3.4.1.1 LVDS Panel Configuration



Options Summary		
LVDS/eDP	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disabled this panel.		
LVDS Panel Type	640X480@60HZ	
	800X480@60HZ	
	800X600@60HZ	
	1024X600@60HZ	
	1024X768@60HZ	Optimal Default, Failsafe Default
	1280X768@60HZ	
	1280X800@60HZ	
	1280X1024@60HZ	
	1366X768@60HZ	
	1440X900@60HZ	
	1600X1200@60HZ	
	1920X1080@60HZ	
	1920X1200@60HZ	

Options Summary		
Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.		
Color Depth	18-bit	Optimal Default, Failsafe Default
	24-bit	
	36-bit	
	48-bit	
Select panel type		
Backlight Mode	BIOS & Application	
	Windows Slider	Optimal Default, Failsafe Default
Select backlight control signal type		
Backlight Type	Normal	Optimal Default, Failsafe Default
	Inverted	
Select backlight control signal type		
Backlight Level	0%	
	10%	
	20%	
	30%	
	40%	
	50%	
	60%	
	70%	
	80%	Optimal Default, Failsafe Default
	90%	
	100%	
Select backlight control level		
Backlight PWM Freq	100Hz	
	200Hz	
	220Hz	Optimal Default, Failsafe Default
	500Hz	
	1.1KHz	
	2.2KHz	
	6.5KHz	
Select PWM frequency of backlight control signal		
Swing Level	150mV	
	200mV	
	250mV	
	300mV	Optimal Default, Failsafe Default
	350mV	
	400mV	

Options Summary		
Swing Level	450mV	
Select Swing Level		
Center Spreading Depth	no spreading	Optimal Default, Failsafe Default
	0.5%	
	1.0%	
	1.5%	
	2.0%	
	2.5%	
Select Center Spreading Depth		

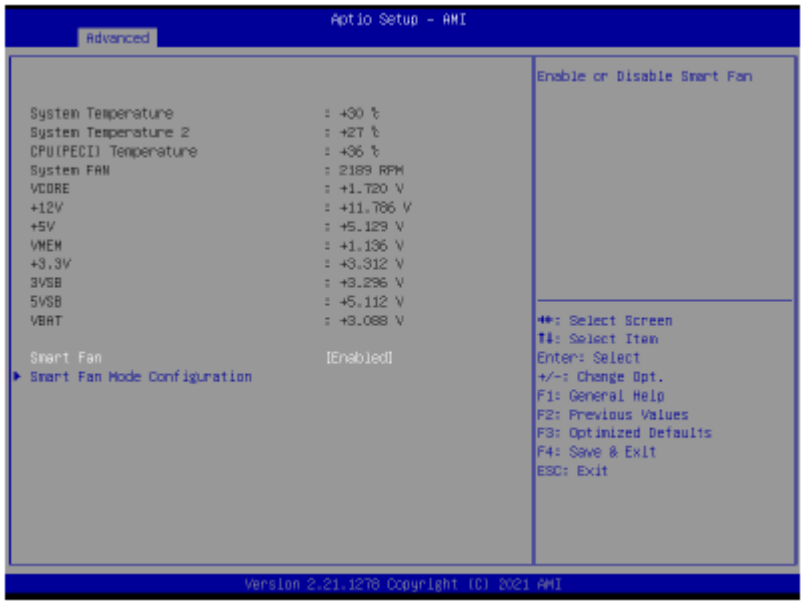
Options Summary		
Platform Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or disable Platform Hierarchy		
Storage Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Storage Hierarchy		
Endorsement Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Endorsement Hierarchy		
TPM2.0 UEFI Spec Version	TCG_1_2	
	TCG_2	Optimal Default, Failsafe Default
Select the TCG2 Spec Version Support, TCG_1_2: Compatible mode for Win8/Win10 TCG_2: Support new TCG2 protocol and event format for Win10 or later		
Physical Presence Spec Version	1.2	
	1.3	Optimal Default, Failsafe Default
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.		

3.4.2 CPU Configuration

Options Summary		
Intel (VMX) Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
Intel(R) SpeedStep(tm)	Disabled	
	Enabled	Optimal Default, Failsafe Default
Allows more than two frequency ranges to be supported.		
Turbo Mode	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable processor Turbo Mode (requires EMTTM enabled too). AUTO means enabled.		

3.4.3 Memory Configuration

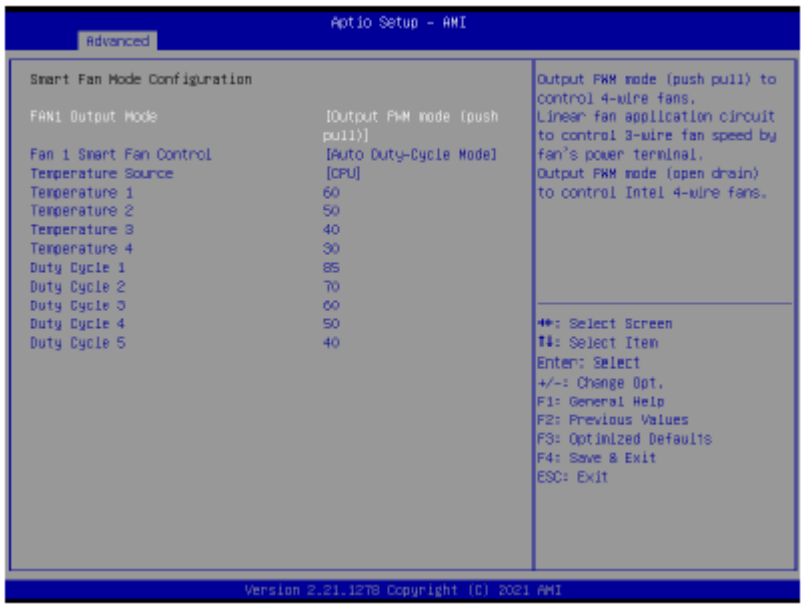
3.4.4 Hardware Monitor



Options Summary		
Smart Fan	Disabled	
	Enabled	Optimal Default; Failsafe Default
Enable or Disable Smart Fan		

3.4.4.1 Smart Fan Mode Configuration

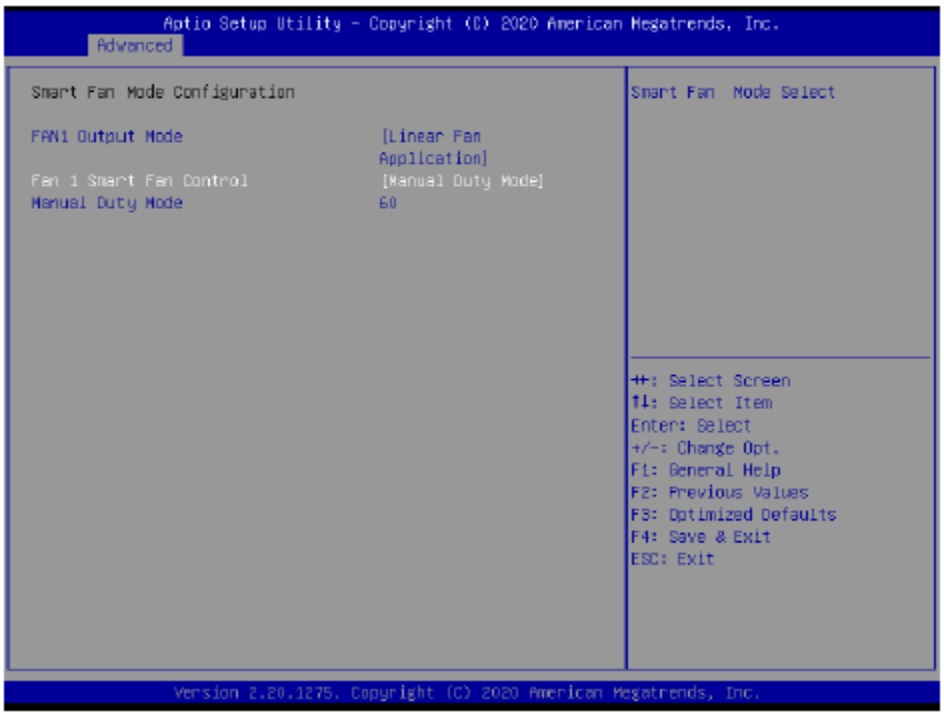
Auto Duty Cycle Mode



Options Summary		
FAN1 Output Mode	Output PWM mode (push pull)	
	Linear Fan Application	
	Output PWM mode (open drain)	Optimal Default, Failsafe Default
Output PWM mode (push pull) to control 4-wire fans.\nLinear fan application circuit to control 3-wire fan speed by fan's power terminal.\nOutput PWM mode (open drain) to control Intel 4-wire fans.		
Fan 1 Smart Fan Control	Manual Duty Mode	
	Auto Duty-Cycle Mode	Optimal Default, Failsafe Default
Smart Fan Mode Select		
Temperature Source	CPU	Optimal Default, Failsafe Default
	System Temperature 2	
	System Temperature	
Select the monitored temperature source for this fan.		

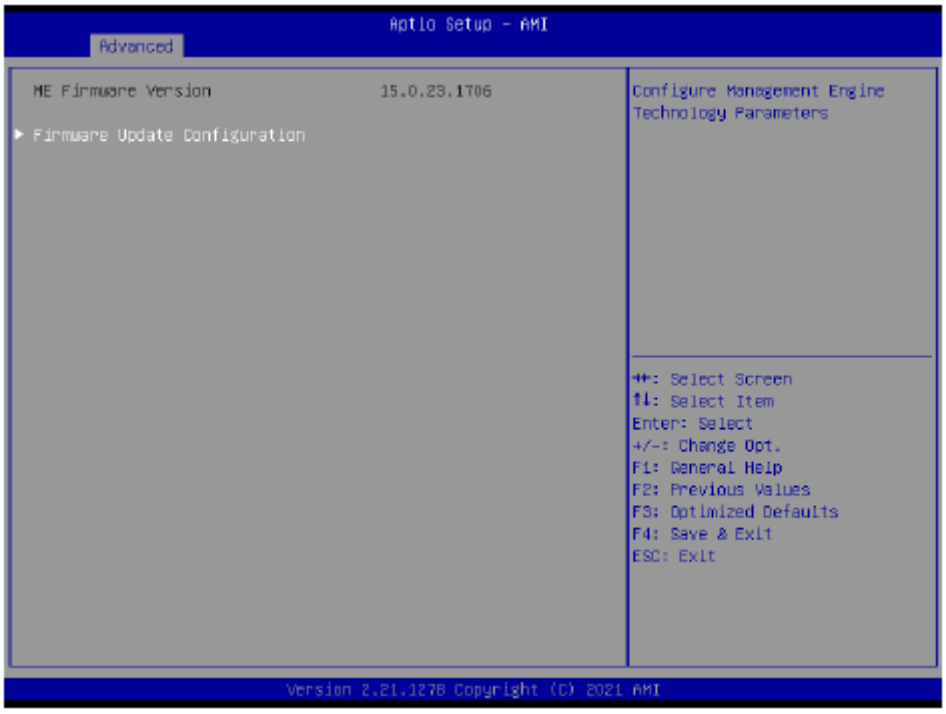
Options Summary	
Duty Cycle	Auto fan speed control. Fan speed will follow different temperature by different duty cycle 1-100
Temperature	

Manual Duty Mode

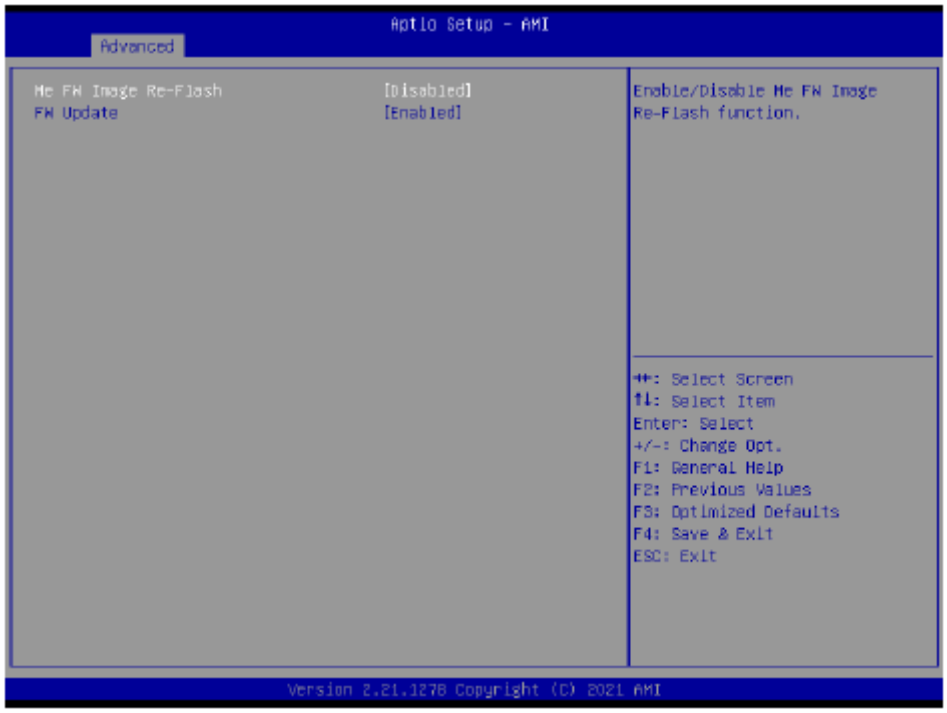


Options Summary		
Manual Duty Mode	60	Optimal Default, Failsafe Default
Manual mode fan control, user can write expected duty cycle (PWM fan type) 1-100		

3.4.5 PCH-FW Configuration



3.4.5.1 Firmware Update Configuration

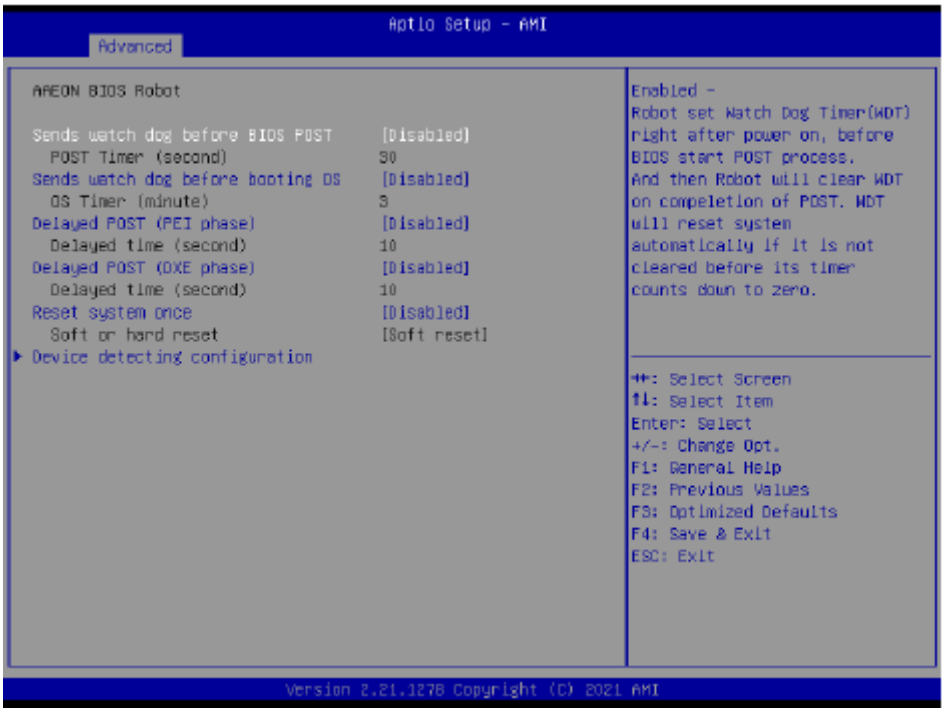


Options Summary		
Me FW Image Re-Flash	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable Me FW Image Re-Flash function.		
FW Update	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable ME FW Update function.		

3.4.6 Power Management

Options Summary		
Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select system power mode		
Restore AC Power Loss	Last State	Optimal Default, Failsafe Default
	Always On	
	Always Off	
IO Restore AC power Loss		
RTC wake system from S5	Disable	Optimal Default, Failsafe Default
	Fixed Time	
	Dynamic Time	
	Bypass	
Fixed Time: System will wake on the hr::min::sec specified./n Dynamic Time: System will wake on the current time + Increase minute(s)./n Bypass: BIOS will not control RTC wake function during system shutdown		

3.4.7 BIOS Robot



Options Summary		
Sends watch dog before BIOS POST	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot set Watch Dog Time r(WDT) right after power on, before BIOS start POST process. Robot will clear WDT on completion of POST. WDT will reset system automatically if it is not cleared before its timer counts down to zero.		
POST Timer (second)	30	Optimal Default, Failsafe Default
Timer count set to Watch Dog Timer for POST. **WARNING**: Do not set to a value equal to or shorter than normal POST time, otherwise system may never complete POST unless clearing BIOS settings. More than twice the normal POST time is suggested.		
Sends watch dog before booting OS	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot set Watch Dog Timer (WDT) after POST completion, before BIOS transfers control to OS. **WARNING**: Before enabling this function, a program in OS must be responsible for clearing WDT. Also, this function should be disabled if OS is going to update itself.		

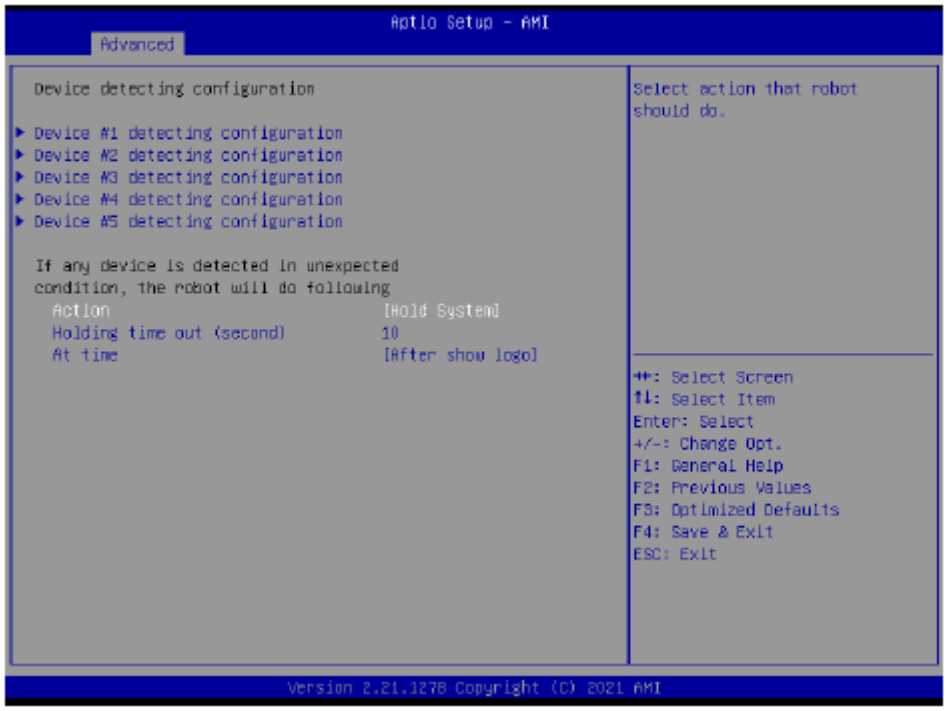
Options Summary		
OS Timer (minute)	3	Optimal Default, Failsafe Default
Timer count set to Watch Dog Timer for OS loading.		
Delayed POST (PEI phase)	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot holds BIOS from starting POST, right after power on. This allows BIOS POST to start with stable power or start after system is physically warmed-up. **Note**: Robot does this before 'Sends watch dog'.		
Delayed time (second)	10	Optimal Default, Failsafe Default
Period of time for Robot to hold BIOS from POST.		
Delayed POST (DXE phase)	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot holds BIOS before POST completion. This allows BIOS POST to start with stable power or start after system is physically warmed-up. **Note**: Robot does this after 'Sends watch dog before BIOS POST'.		
Delayed time (second)	10	Optimal Default, Failsafe Default
Period of time for Robot to hold BIOS from POST.		
Reset system once	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot resets system for one time on each boot. This will send a soft or hard reset to onboard devices, thus puts devices to more stable state.		
Soft or hard reset	Soft reset	Optimal Default, Failsafe Default
	Hard reset	
Select reset type robot should send on each boot.		

3.4.7.1 Device Detecting Configuration

Action: Rest System

Options Summary		
Action	Reset System	Optimal Default, Failsafe Default
	Hold System	
Select action that robot should do.		
Soft or hard reset	Soft	Optimal Default, Failsafe Default
	Hard	
Select reset type robot should send on each boot.		
Retry-Count	3	Optimal Default, Failsafe Default
Fill retry counter here. Robot will reset system at most counter times, and then let system continue its POST.		
At time	After show logo	Optimal Default, Failsafe Default
	Before show logo	
Select robot action time: After show logo – Robot will do action after logo is displayed. System devices are almost ready. Before show logo – Robot will do action earlier before logo, but some devices may not be ready.		

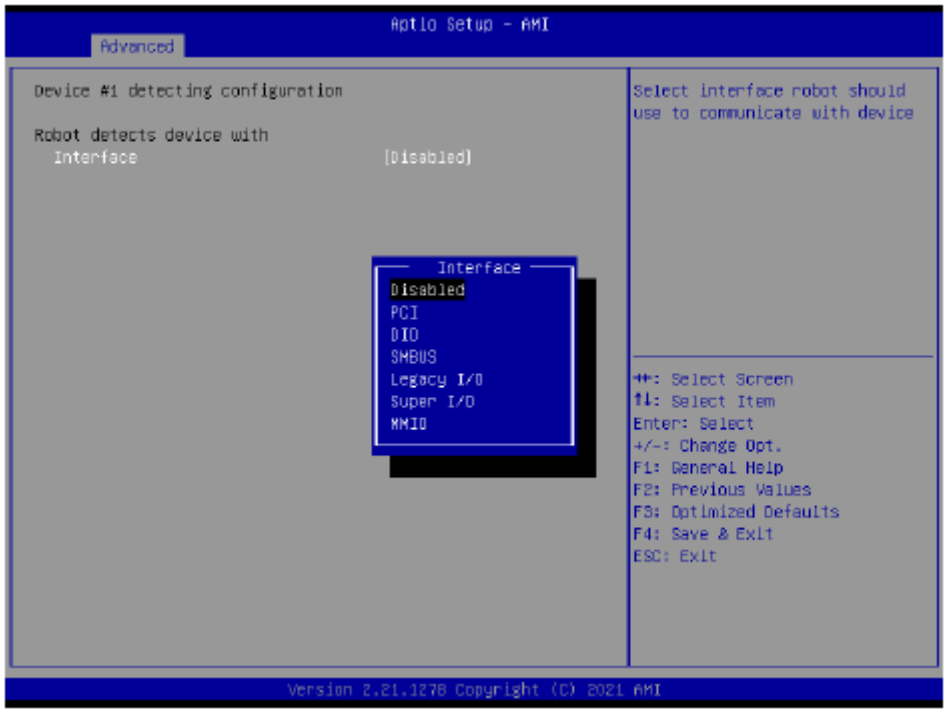
Action: Hold System



Options Summary		
Action	Reset System	Optimal Default, Failsafe Default
	Hold System	
Select action that robot should do.		
Holding time out (second)	10	Optimal Default, Failsafe Default
Fill hold time out here. Robot will hold system no longer then time-out value, and then let system continue its POST.		
At time	After show logo	Optimal Default, Failsafe Default
	Before show logo	
Select robot action time: After show logo - Robot will do actoin after logo is displayed. System devices are almost ready. Before show logo - Robot will do action earlier before logo, but some devices may not be ready.		

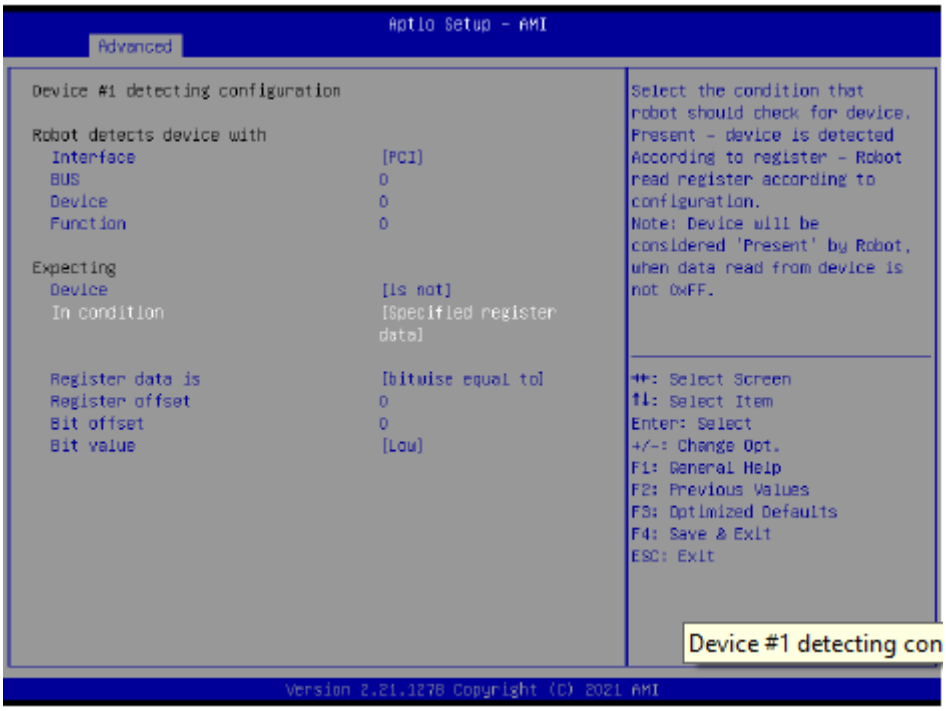
3.4.7.1.1 Device# Detecting Configuration

Interface: Disabled



Options Summary		
Interface	Disabled	Optimal Default, Failsafe Default
	PCI	
	DIO	
	SMBUS	
	Legacy I/O	
	Super I/O	
	MMIO	
Select interface robot should use to communicate with device.		

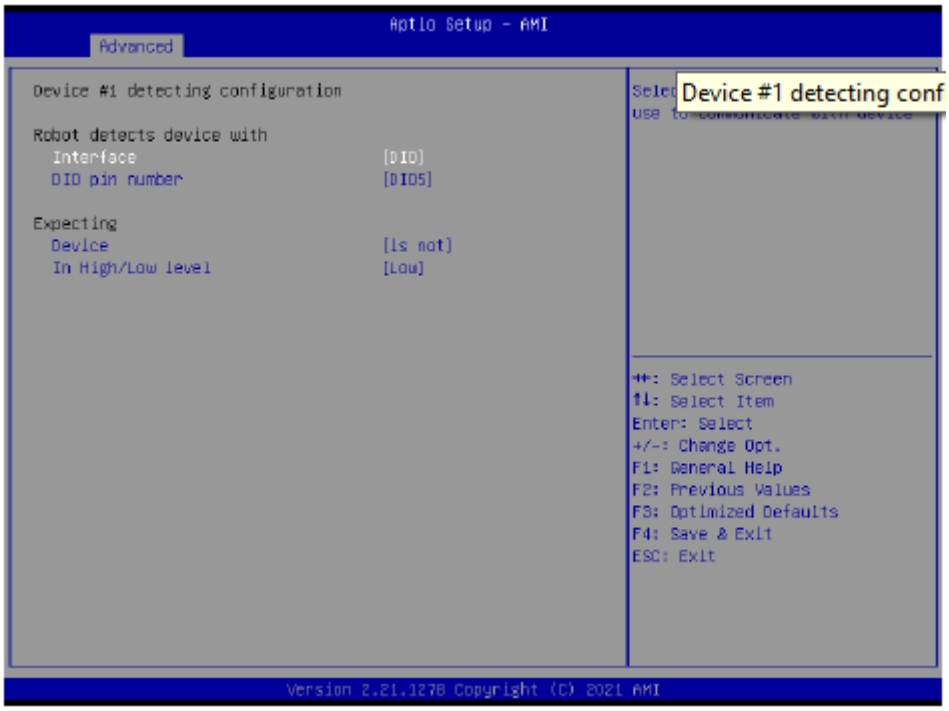
Interface: PCI



Options Summary		
BUS	0	Optimal Default, Failsafe Default
Fill BUS number to a PCI device, in hexadecimal. Range: 0 - FF		
Device	0	Optimal Default, Failsafe Default
Fill DEVICE number to a PCI device, in hexadecimal. Range: 0 - FF		
Function	0	Optimal Default, Failsafe Default
Fill FUNCTION number to a PCI device, in hexadecimal. Range: 0 - FF		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select that robot should or should not do action if condition met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected According to register - Robot read register according to configuration. **Note**: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		

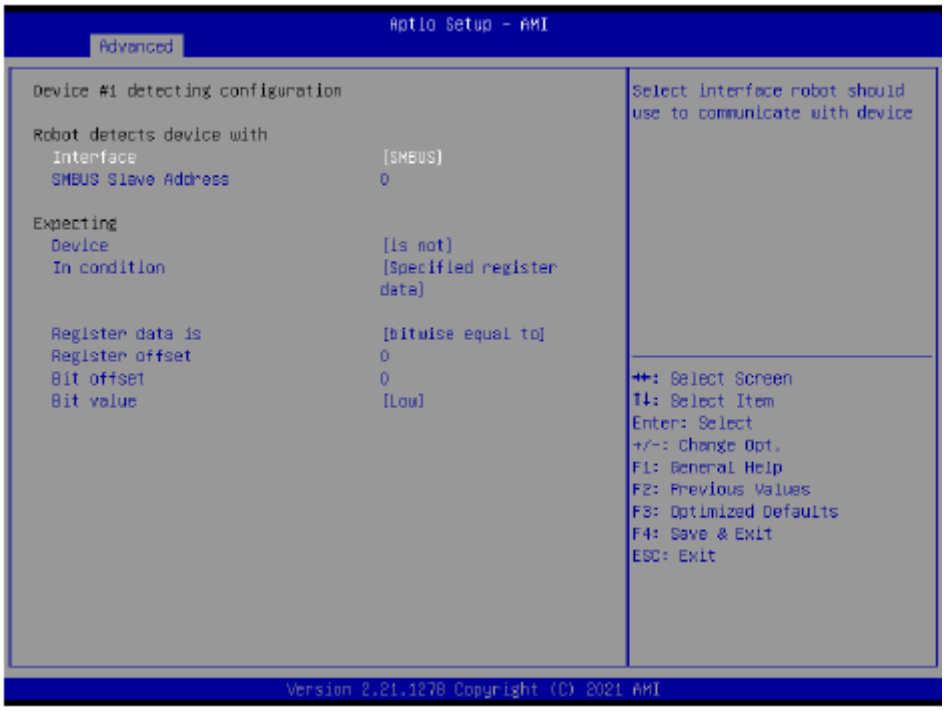
Options Summary		
Register data is	bitwise equal to	Optimal Default, Failsafe Default
	bytewise equal to	
	bytewise lesser than	
	bytewise larger than	
Select how robot should compare data read from register, to a value configured below.		
Register offset	0	Optimal Default, Failsafe Default
Fill register offset (or index) for robot to read, in hexadecimal. Range: 0 - FF		
Bit offset	0	Optimal Default, Failsafe Default
Fill bit offset for register, for robot to compare with bit value.		
Bit value	Low	Optimal Default, Failsafe Default
	High	
Fill bit value for robot to compare register-bit with specified offset.		
Byte value	0	Optimal Default, Failsafe Default
Fill a byte value for robot to compare register data with, in hexadecimal. Range: 0 - FF		

Interface: DIO



Options Summary		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select that robot should or should not do action if condition met.		
DIO pin number	DIO1	Optimal Default, Failsafe Default
	DIO*	
Fill DIO pin number. 0 - DIO0, 1 - DIO1, and so on. For COM express product: 0-3 - GPI0-3, 4-7 - GPO0-3		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select that robot should or should not do action if condition met.		
In High/Low level	Low	Optimal Default, Failsafe Default
	High	
Select High/Low level of the DIO pin that robot should do action.		

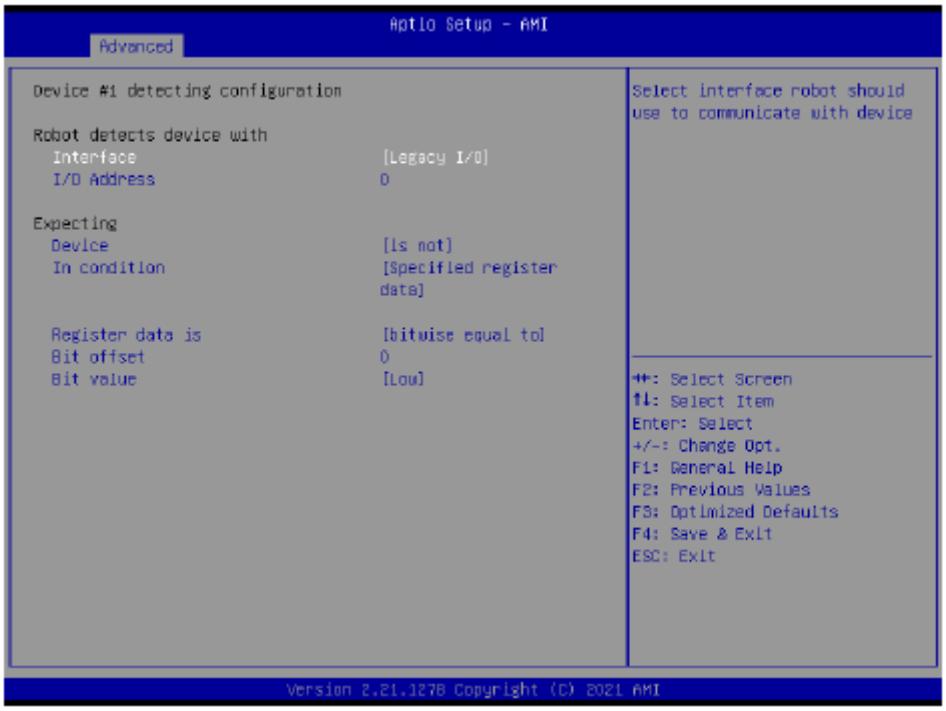
Interface: SMBUS



Options Summary		
SMBUS Slave Address	0	Optimal Default, Failsafe Default
Fill slave address to a SMBUS device, in hexadecimal. Range: 0 - FF		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select that robot should or should not do action if condition met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected According to register - Robot read register according to configuration. **Note**: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		
Register data is	bitwise equal to	Optimal Default, Failsafe Default
	bytewise equal to	
	bytewise lesser than	
	bytewise larger than	
Select how robot should compare data read from register, to a value configured below.		

Options Summary		
Register offset	0	Optimal Default, Failsafe Default
Fill register offset (or index) for robot to read, in hexadecimal. Range: 0 - FF		
Bit offset	0	Optimal Default, Failsafe Default
Fill bit offset for register, for robot to compare with bit value.		
Bit value	Low	Optimal Default, Failsafe Default
	High	
Fill bit value for robot to compare register-bit with specified offset.		
Byte value	0	Optimal Default, Failsafe Default
Fill a byte value for robot to compare register data with, in hexadecimal. Range: 0 - FF		

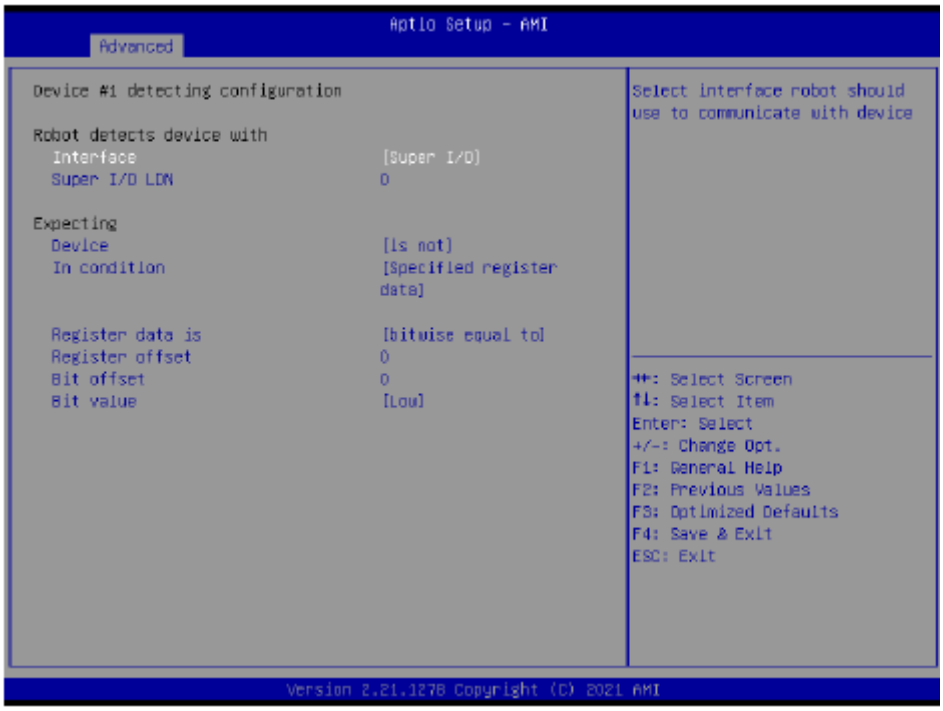
Interface: Legacy I/O



Options Summary		
I/O Address	0	Optimal Default, Failsafe Default
Fill I/O address device is responding to. Range: 0~FFFF		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select that robot should or should not do action if condition met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected According to register - Robot read register according to configuration. **Note**: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		
Register data is	bitwise equal to	Optimal Default, Failsafe Default
	bytewise equal to	
	bytewise lesser than	
	bytewise larger than	
Select how robot should compare data read from register, to a value configured below.		

Options Summary		
Bit offset	0	Optimal Default, Failsafe Default
Fill bit offset for register, for robot to compare with bit value.		
Bit value	Low	Optimal Default, Failsafe Default
	High	
Fill bit value for robot to compare register-bit with specified offset.		
Byte value	0	Optimal Default, Failsafe Default
Fill a byte value for robot to compare register data with, in hexadecimal. Range: 0 - FF		

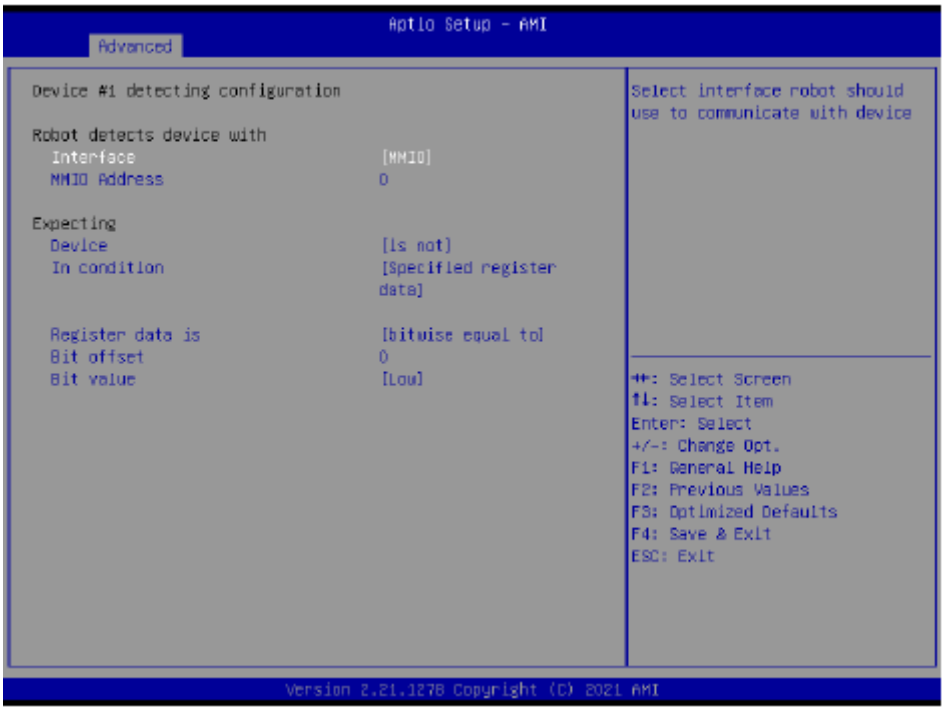
Interface: Super I/O



Options Summary		
Super I/O LDN	0	Optimal Default, Failsafe Default
Fill LDN number to a Super I/O device. Range: 0~FF		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select that robot should or should not do action if condition met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected According to register - Robot read register according to configuration. **Note**: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		
Register data is	bitwise equal to	Optimal Default, Failsafe Default
	bytewise equal to	
	bytewise lesser than	
	bytewise larger than	
Select how robot should compare data read from register, to a value configured below.		

Options Summary		
Register offset	0	Optimal Default, Failsafe Default
Fill register offset (or index) for robot to read, in hexadecimal. Range: 0 - FF		
Bit offset	0	Optimal Default, Failsafe Default
Fill bit offset for register, for robot to compare with bit value.		
Bit value	Low	Optimal Default, Failsafe Default
	High	
Fill bit value for robot to compare register-bit with specified offset.		
Byte value	0	Optimal Default, Failsafe Default
Fill a byte value for robot to compare register data with, in hexadecimal. Range: 0 - FF		

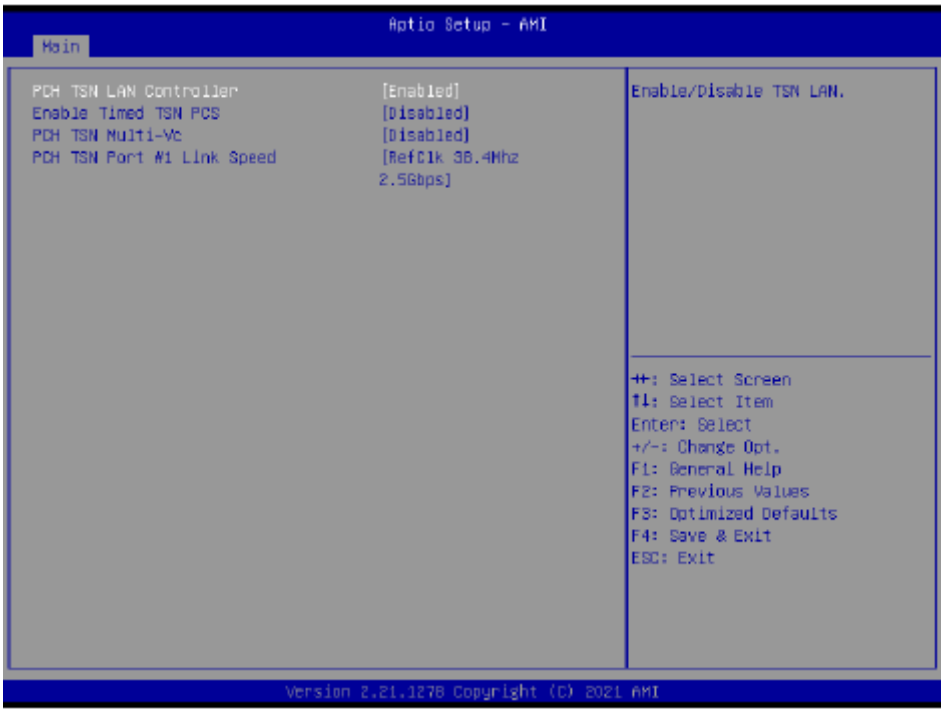
Interface: MMIO



Options Summary		
MMIO Address	0	Optimal Default, Failsafe Default
Fill Memory Mapped I/O address device is responding to. Range: 0~FFFFFFFF		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select that robot should or should not do action if condition met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected According to register - Robot read register according to configuration. **Note**: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		
Register data is	bitwise equal to	Optimal Default, Failsafe Default
	bytewise equal to	
	bytewise lesser than	
	bytewise larger than	
Select how robot should compare data read from register, to a value configured below.		

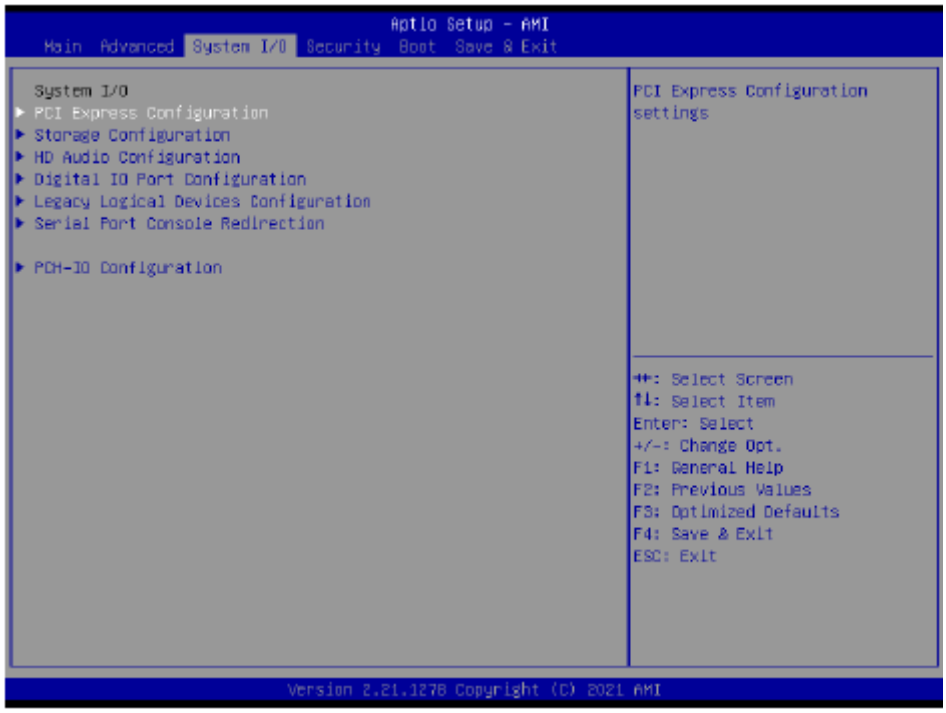
Options Summary		
Bit offset	0	Optimal Default, Failsafe Default
Fill bit offset for register, for robot to compare with bit value.		
Bit value	Low	Optimal Default, Failsafe Default
	High	
Fill bit value for robot to compare register-bit with specified offset.		
Byte value	0	Optimal Default, Failsafe Default
Fill a byte value for robot to compare register data with, in hexadecimal. Range: 0 - FF		

3.4.8 TSN GBE Configuration

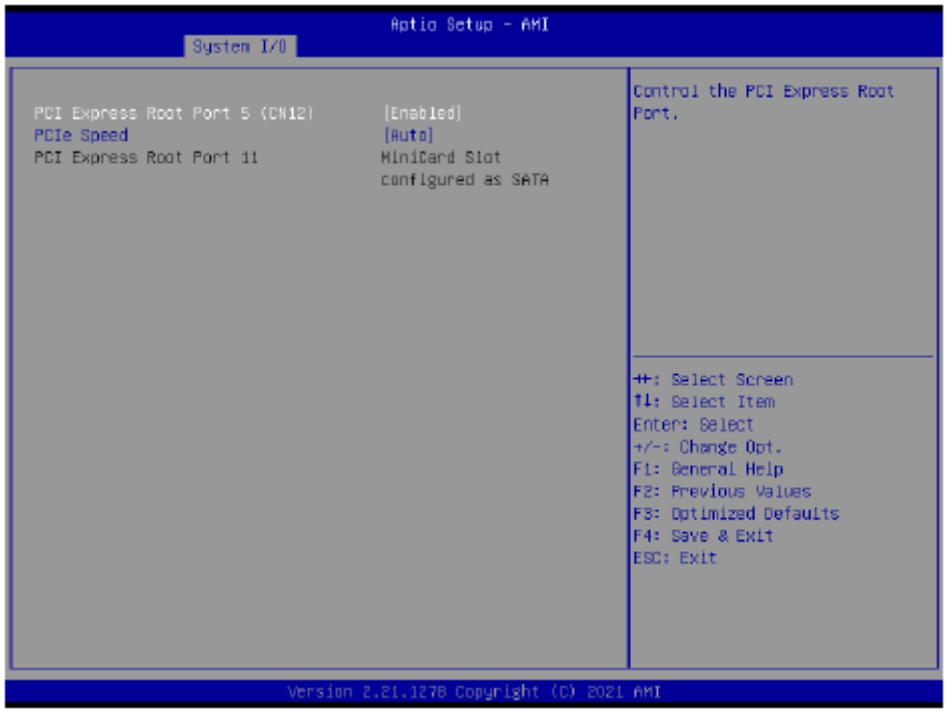


Options Summary		
PCH TSN LAN Controller	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable/Disable TSN LAN		
Enable Timed TSN PCS	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable TSN PCS. When enabled, TSN PCS device will appear in ACPI table		
PCH TSN Multi-Vc	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable PCH TSN Multi Virtual Channels		
PCH TSN Port #1 Link Speed	RefClk 24Mhz 2.5Gbps	
	RefClk 24Mhz 1Gbps	Optimal Default, Failsafe Default
	RefClk 38.4Mhz 2.5Gbps	
	RefClk 38.4Mhz 1Gbps	
PCH TSN Link Speed config		

3.5 Setup Submenu: System I/O

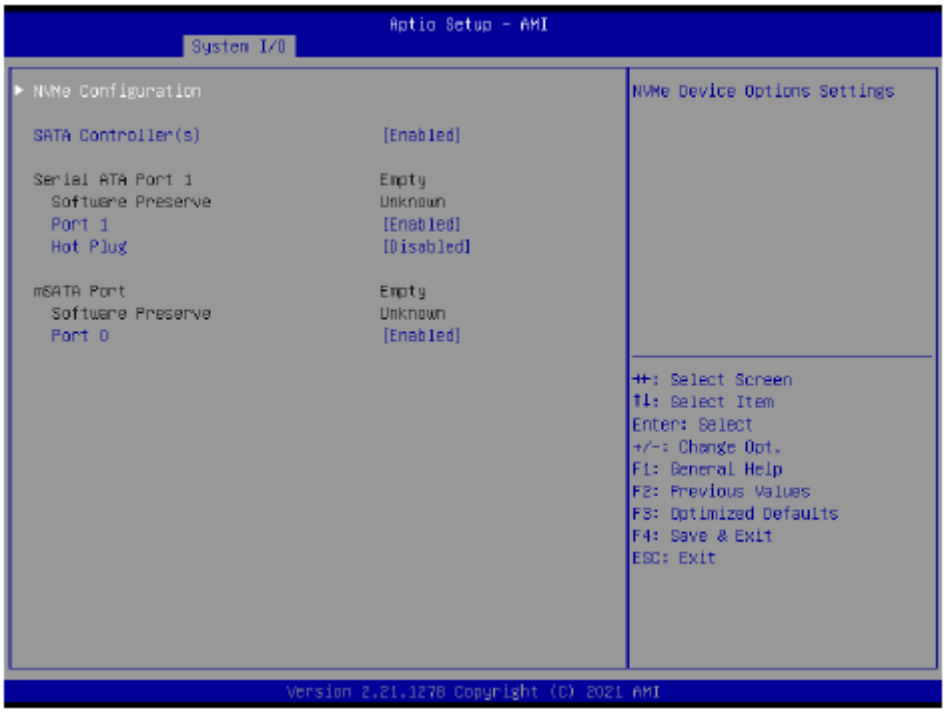


3.5.1 PCI Express Configuration



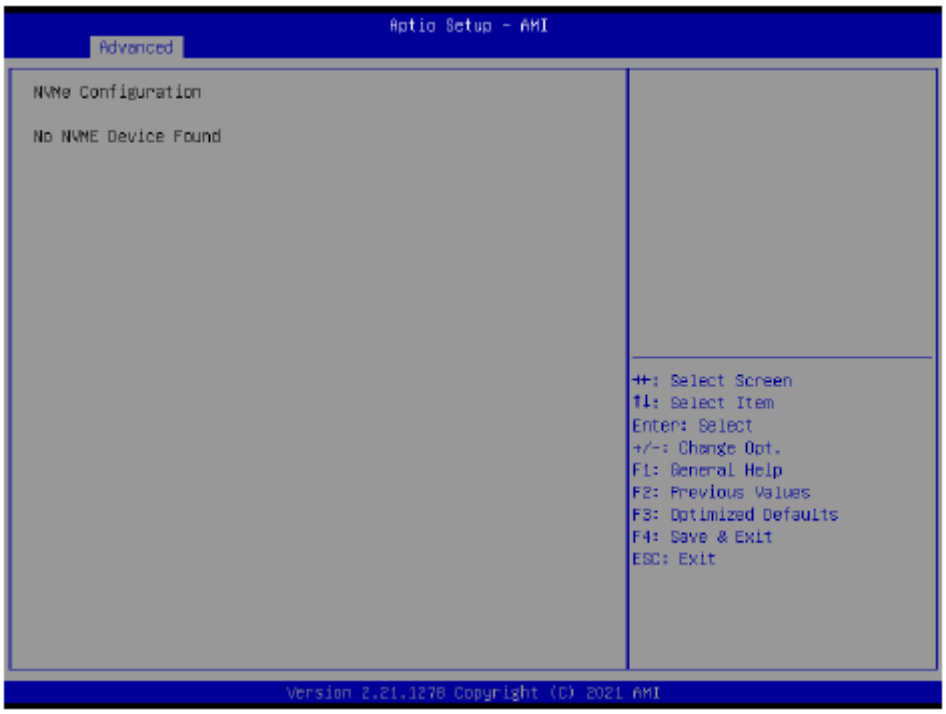
Options Summary		
PCI Express Root Port 5 (CN12) / Port11	Enabled	Optimal Default, Failsafe Default
	Disabled	
Control the PCI Express Root Port.		
PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
Control the PCI Express Speed		

3.5.2 Storage Configuration

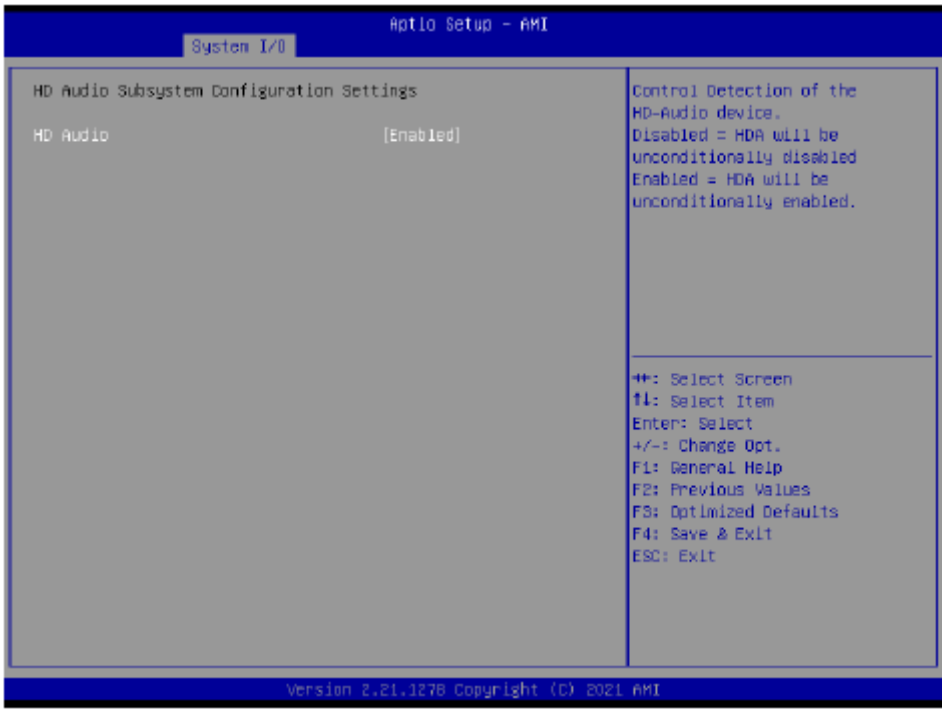


Options Summary		
SATA Controller(s)	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable SATA Device.		
Port 0 / 1	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port		
Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
Designates this port as Hot Pluggable.		

3.5.2.1 NVME Configuration

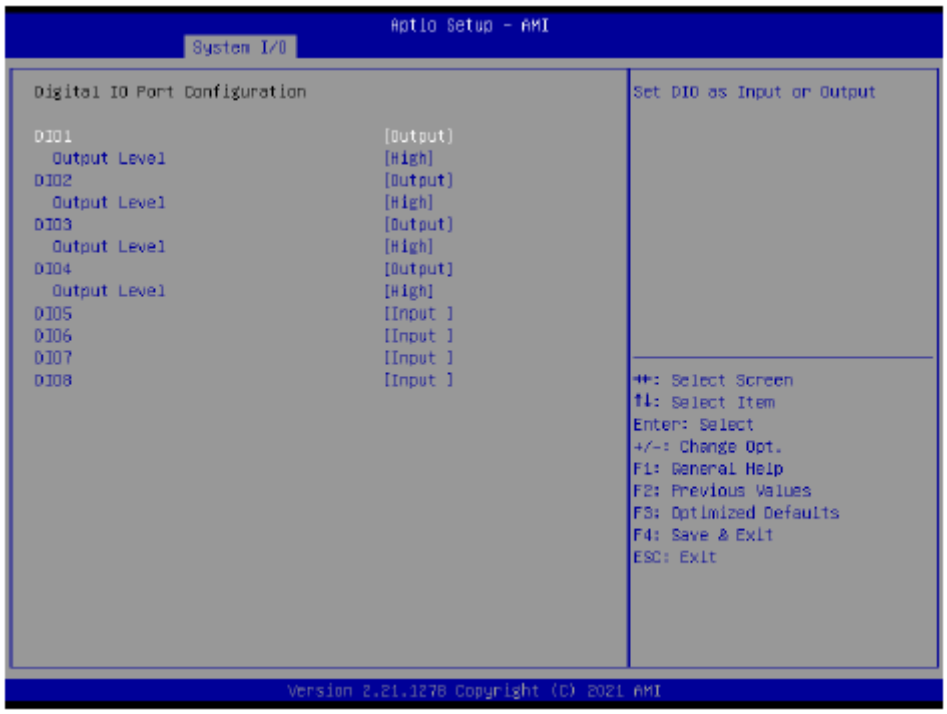


3.5.3 HD Audio Subsystem Configuration Settings



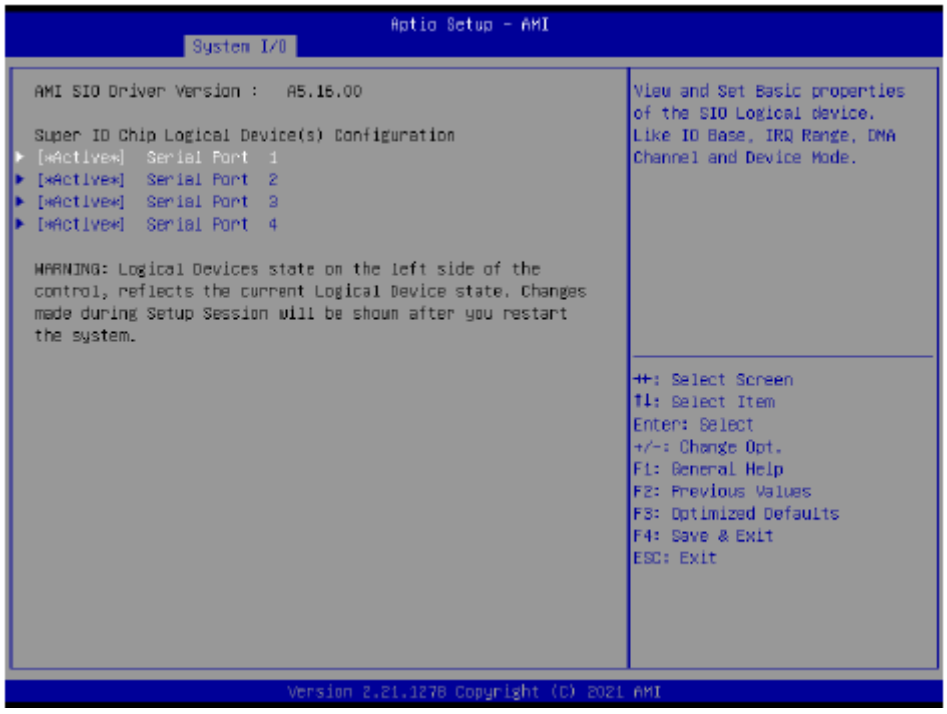
Options Summary		
HD Audio	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled Enabled = HDA will be unconditionally enabled.		

3.5.4 Digital IO Port Configuration

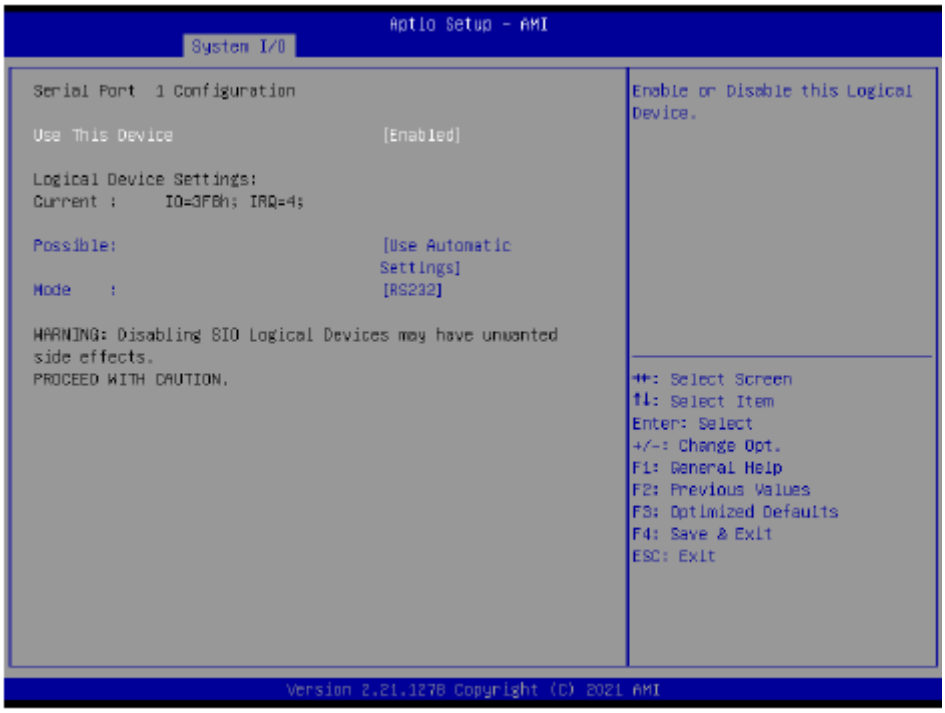


Options Summary		
DIO Port #	Output	
	Input	
Set DIO as Input or Output		
Output Level	High	Optimal Default, Failsafe Default
	Low	
Set output level when DIO pin is output		

3.5.5 Legacy Logical Devices Configuration

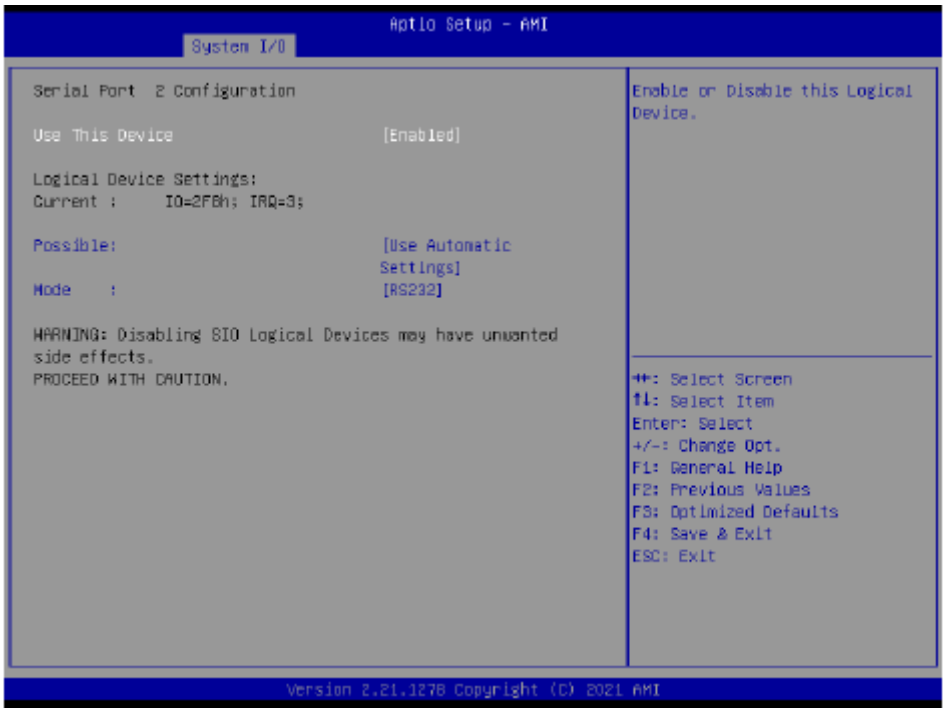


3.5.5.1 Serial Port1 Configuration



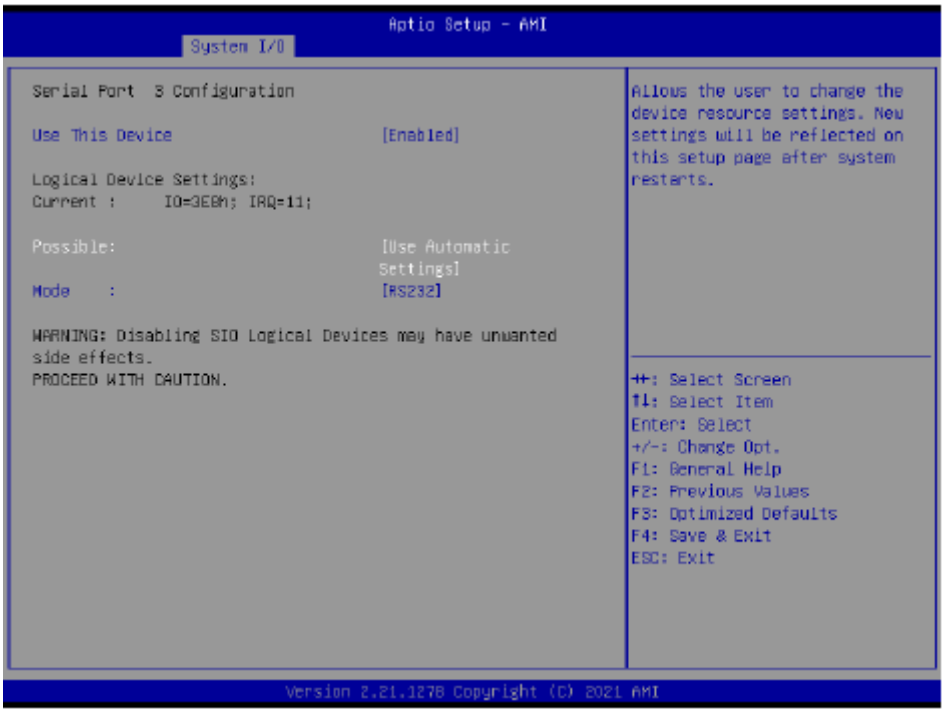
Options Summary		
Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8h; IRQ=4	
	IO=2F8h; IRQ=3	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection		

3.5.5.2 Serial Port2 Configuration



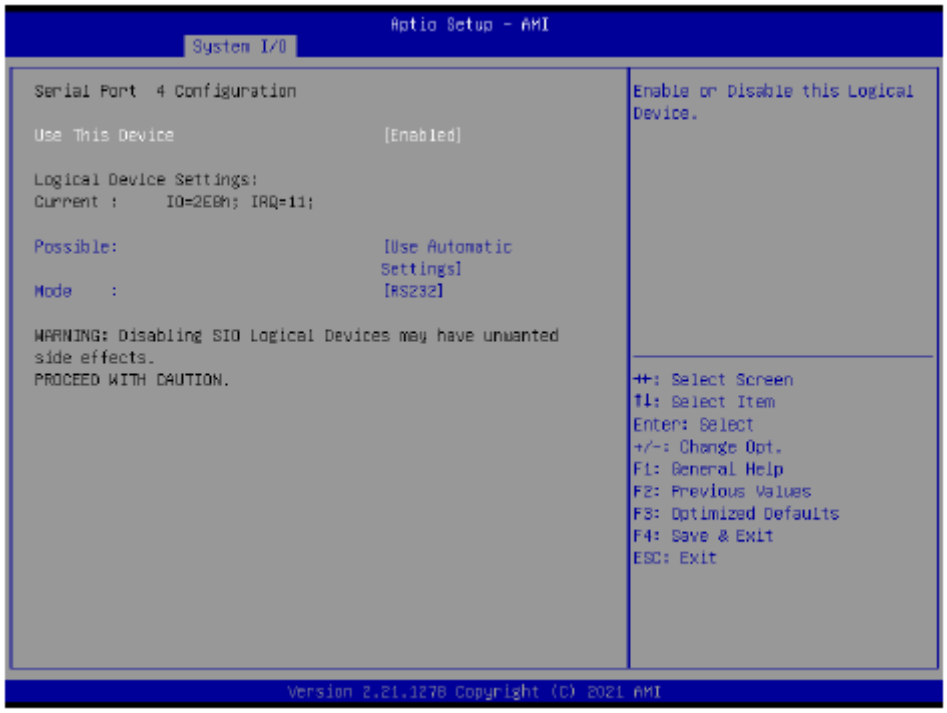
Options Summary		
Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8h; IRQ=3	
	IO=3F8h; IRQ=4	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection		

3.5.5.3 Serial Port3 Configuration



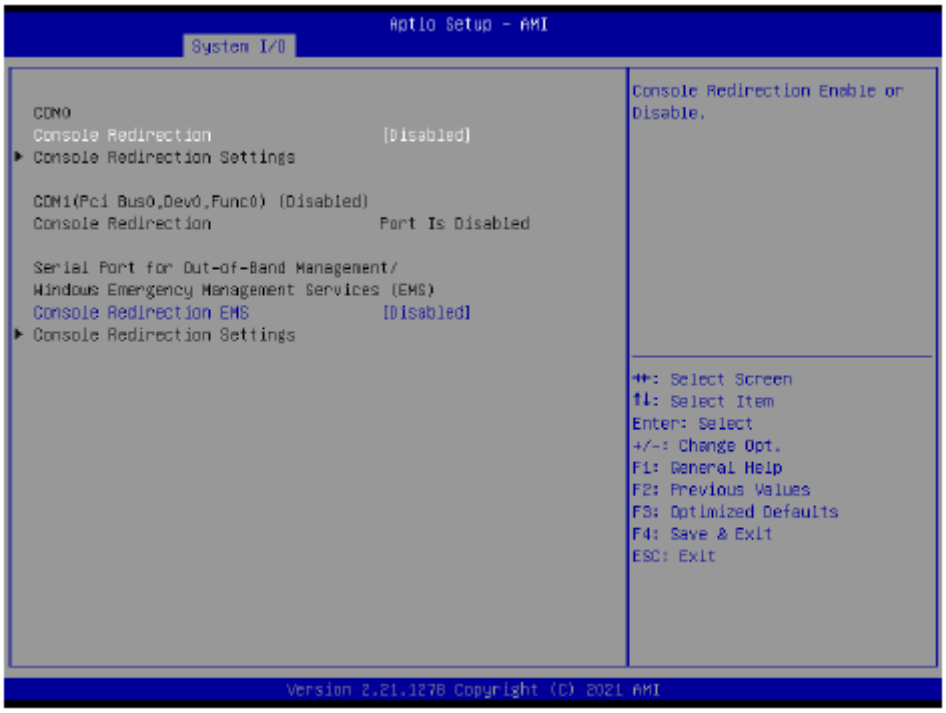
Options Summary		
Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3E8h; IRQ=11	
	IO=2E8h; IRQ=11	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection		

3.5.5.4 Serial Port4 Configuration



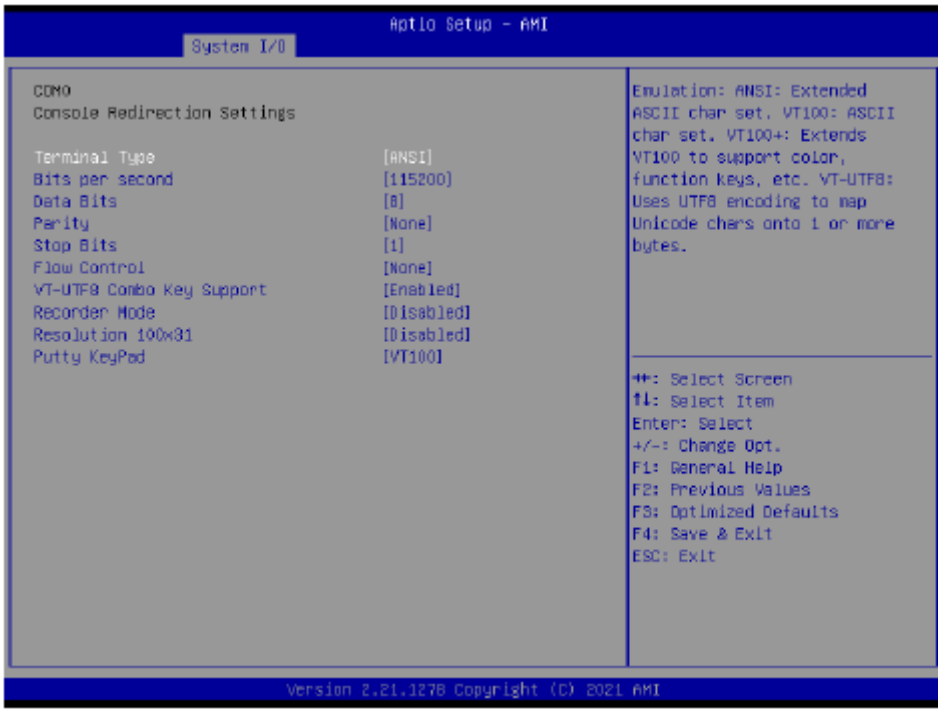
Options Summary		
Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2E8h; IRQ=11	
	IO=3E8h; IRQ=11	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection		

3.5.6 Legacy Logical Devices Configuration



Options Summary		
Console Redirection	Disabled	Optimal Default, Failsafe Default
	Enabled	
Console Redirection Enable or Disable.		
Console Redirection EMS	Disabled	Optimal Default, Failsafe Default
	Enabled	
Console Redirection Enable or Disable.		

3.5.6.1 Console Redirection Settings



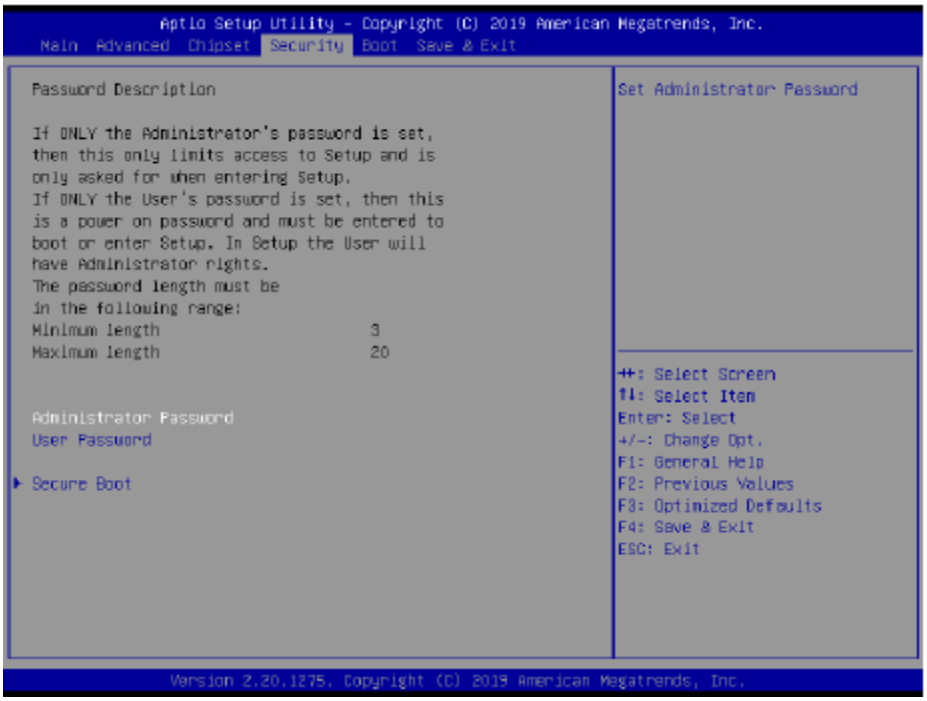
Options Summary		
Terminal Type	VT100	
	VT100+	
	VT-UTF8	
	ANSI	Optimal Default, Failsafe Default
Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.		
Bits Per second	9600	
	19200	
	38400	
	57600	
	115200	Optimal Default, Failsafe Default
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.		
Data Bits	7	
	8	Optimal Default, Failsafe Default
Data Bits		

Options Summary		
Parity	None	Optimal Default, Failsafe Default
	Even	
	Odd	
	Mark	
	Space	
A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.		
Stop Bits	1	Optimal Default, Failsafe Default
	2	
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.		
Flow Control	None	Optimal Default, Failsafe Default
	Hardware RTS/CTS	
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.		
VT-UTF8 Combo Key Support	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals		
Recorder Mode	Disabled	Optimal Default, Failsafe Default
	Enabled	
With this mode enabled only text will be sent. This is to capture Terminal data.		
Resolution 100x31	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enables or disables extended terminal resolution		
Putty KeyPad	VT100	Optimal Default, Failsafe Default
	LINUX	
	XTERMR6	
	SCO	
	ESCN	
	VT400	
Select FunctionKey and KeyPad on Putty.		

3.5.7 PCH-IO Configuration

Options Summary		
MiniCard Slot Function	SATA	Optimal Default, Failsafe Default
	PCIe	
Select function enabled for Full size MiniCard Slot (CN10)		

3.6 Setup Submenu: Security



Change User/Administrator Password

You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, and press Enter. In the dialog box, enter your password (must be between 3 and 20 letters or numbers). Press Enter and retype your password to confirm. Press Enter again to set the password.

Removing the Password

Select the password you want to remove and enter the current password. At the next dialog box press Enter to disable password protection.

3.6.1 Trusted Computing

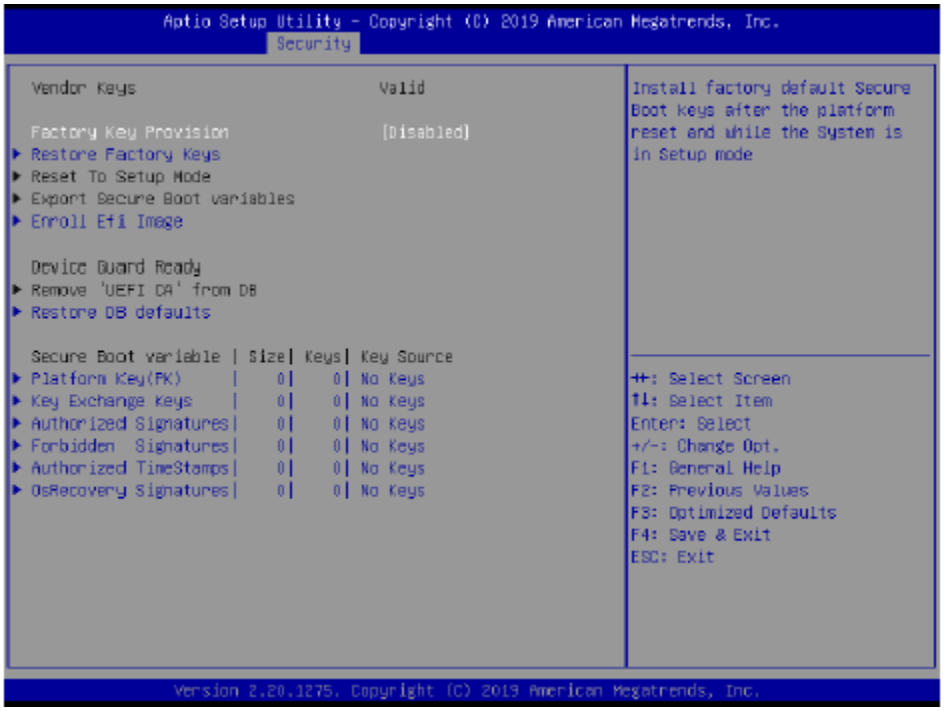
Options Summary		
Security Device Support	Disable	
	Enable	Optimal Default, Failsafe Default
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
SHA-1 PCR Bank	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable SHA-1 PCR Bank		
SHA256 PCR Bank	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable SHA256 PCR Bank		
Pending Operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.		

Options Summary		
Platform Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or disable Platform Hierarchy		
Storage Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Storage Hierarchy		
Endorsement Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Endorsement Hierarchy		
TPM2.0 UEFI Spec Version	TCG_1_2	
	TCG_2	Optimal Default, Failsafe Default
Select the TCG2 Spec Version Support, TCG_1_2: the Compatible mode for Win8/Win10 TCG_2: Support new TCG2 protocol and event format for Win10 or later		
Physical Presence Spec Version	1.2	
	1.3	Optimal Default, Failsafe Default
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.		

3.6.2 Secure Boot

Options Summary		
Secure Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset		
Secure Boot Mode	Custom	Optimal Default, Failsafe Default
	Standard	
Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication		
Restore Factory Keys		
Force System to User Mode. Install factory default Secure Boot key databases		
Reset To Setup Mode		
Delete all Secure Boot key databases from NVRAM		

3.6.2.1 Key Management



Options Summary		
Factory Key Provision	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset		
Restore Factory Keys		
Force System to User Mode. Install factory default Secure Boot key databases		
Reset To Setup Mode		
Delete all Secure Boot key databases from NVRAM		
Export Secure Boot variables		
Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device		
Enroll Efi Image		
Allow the image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db)		

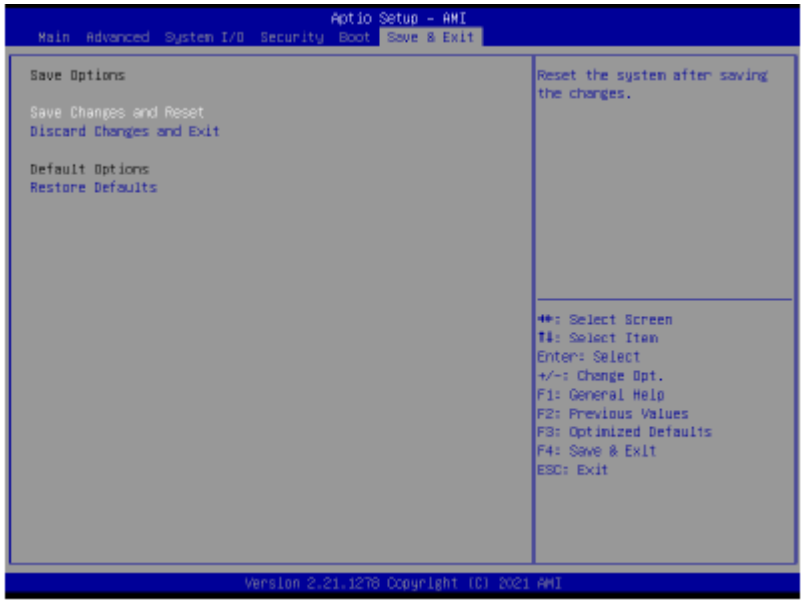
Options Summary		
Remove 'UEFI CA' from DB		
Device Guard ready system must not list 'Microsoft UEFI CA' Certificate in Authorized Signature database (db)		
Restore DB defaults		
Restore DB variable to factory defaults		
Platform Key(PK)	Details	
	Export	
	Update	
	Delete	
Key Exchange Keys	Details	
	Export	
	Update	
	Append	
	Delete	
Authorized Signatures	Details	
	Export	
	Update	
	Append	
	Delete	
Forbidden Signatures	Details	
	Export	
	Update	
	Append	
	Delete	
Authorized TimeStamps	Update	
	Append	
OsRecovery Signatures	Update	
	Append	
Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate: a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER) c) EFI_CERT_RSA2048 (bin) d) EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image (SHA256) Key Source: Factory, External, Mixed		

3.7 Setup Submenu: Boot

Options Summary		
Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables or disables showing boot logo.		
Network Stack	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable UEFI Network Stack		

3.7.1 BBS Priorities

3.8 Setup Submenu: Save & Exit

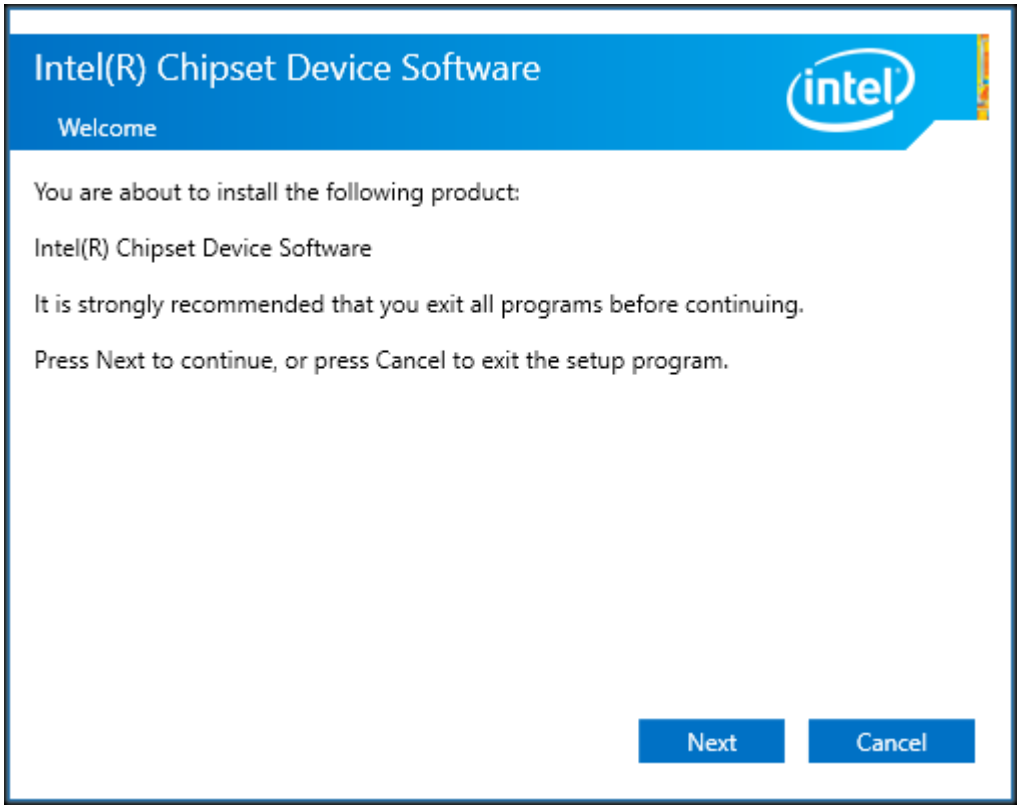


Chapter 4 Installation of Drivers

4.1 Intel® Chipset Device Software

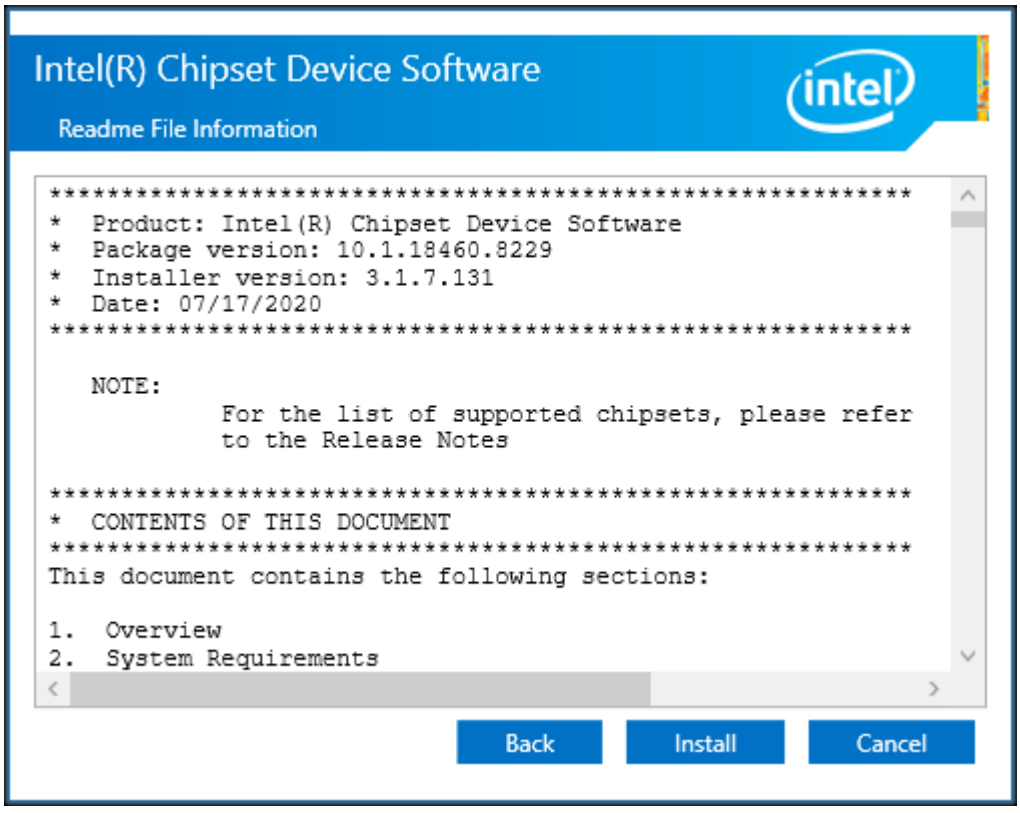
To install the Intel® Chipset Device Software, please follow the steps below.

Step 1. Here is welcome page. Please make sure you save and exit all programs before install**.** Click **Next.**



Step2. Read the license agreement. Click **Accept** to accept all of the terms of the license agreement.

Step3. Click **Install** to begin the installation.



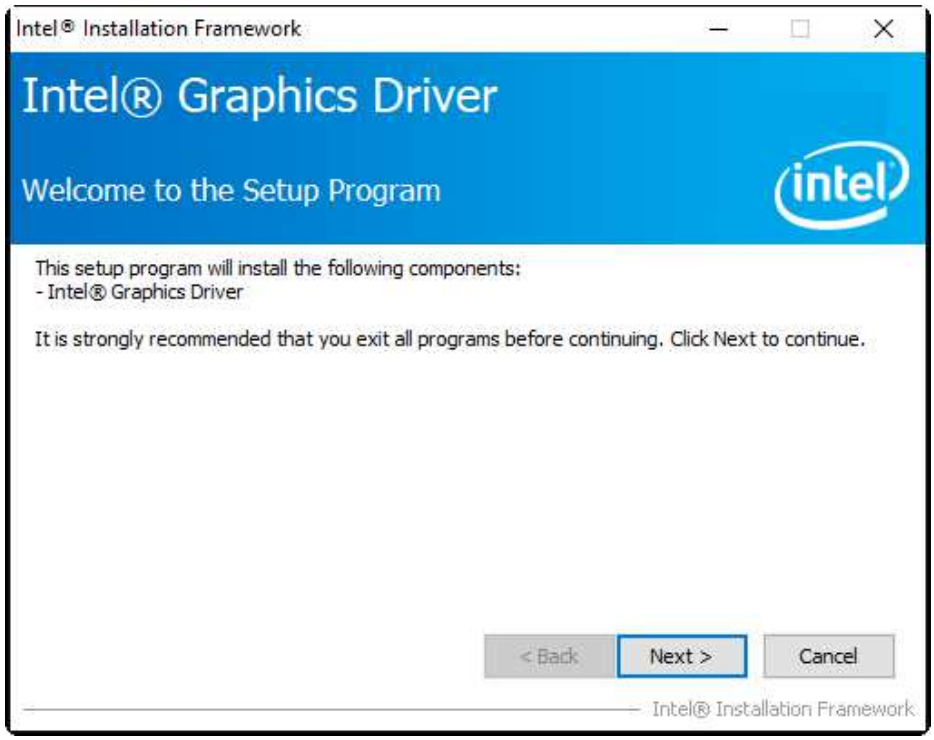
Step5. Click **Finish** to finish installation.


Intel(R) Chipset Device Software
Completion
You have successfully installed the following product:
Intel(R) Chipset Device Software
Press Finish to complete the setup process.
View Log Files
Finish

4.2 Intel® VGA Chipset

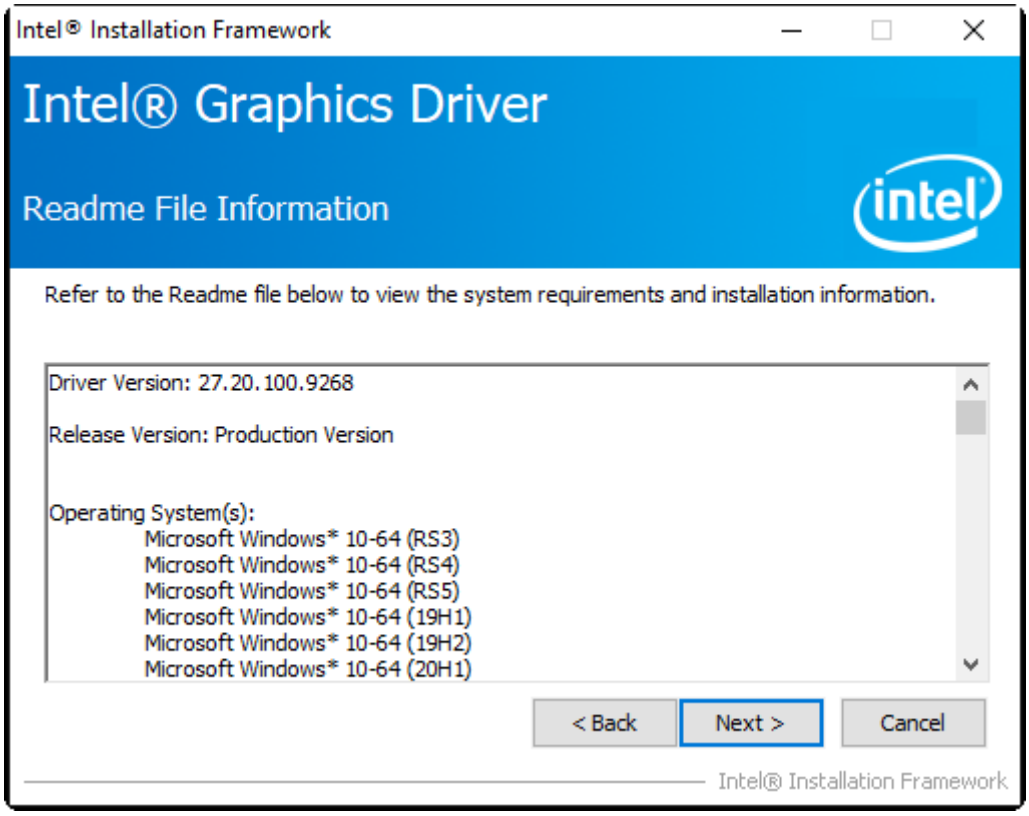
To install the Intel® VGA Chipset, please follow the steps below.

Step1. Click **Next.**

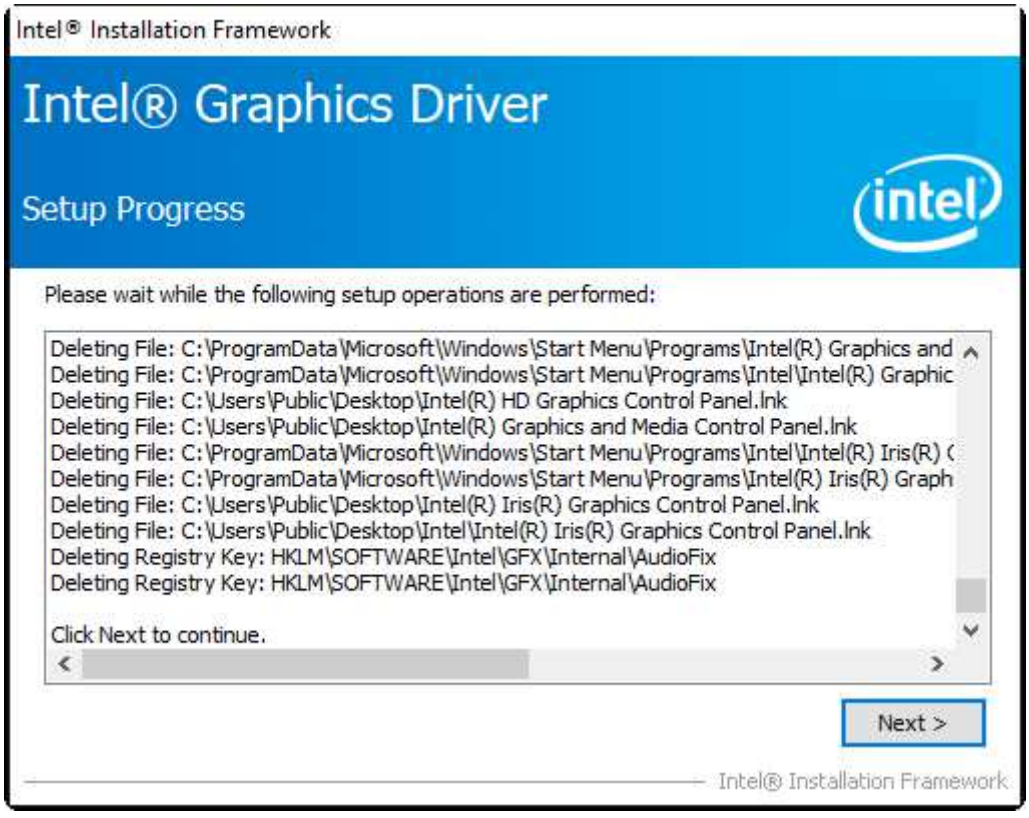


Step2. Read the license agreement. Click **Yes** to accept all of the terms of the license agreement.

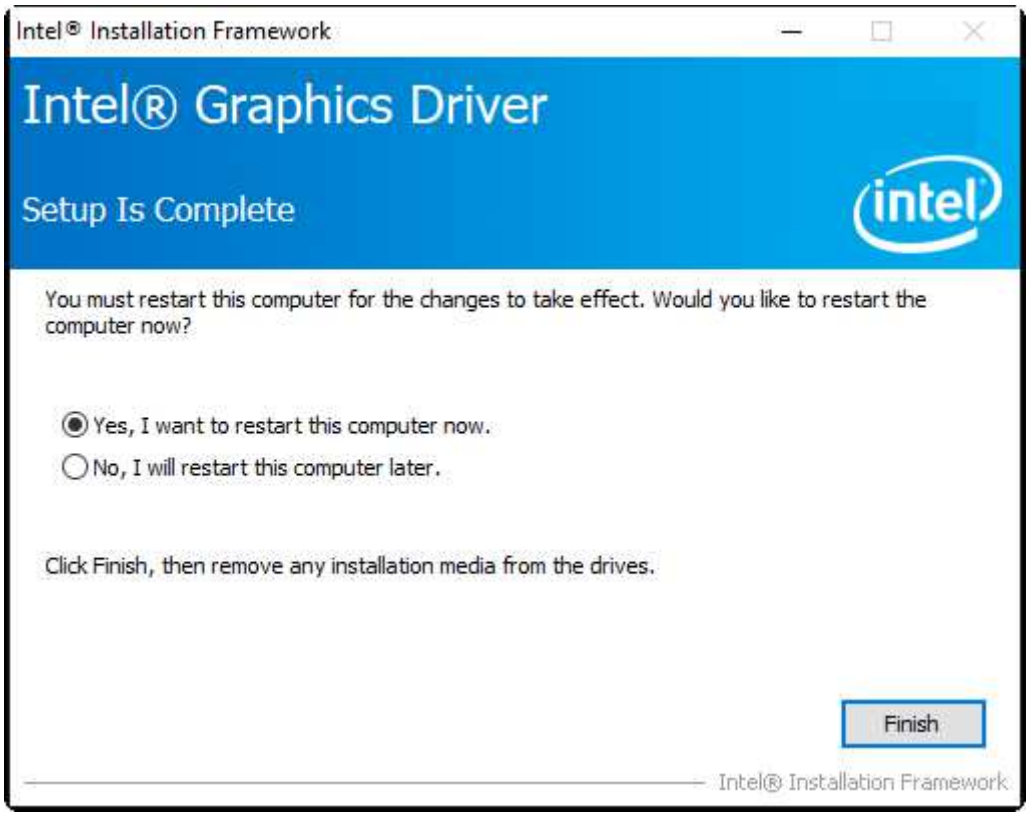
Step3. Click **Next** to continue.



Step4. Click **Next** to continue the program.



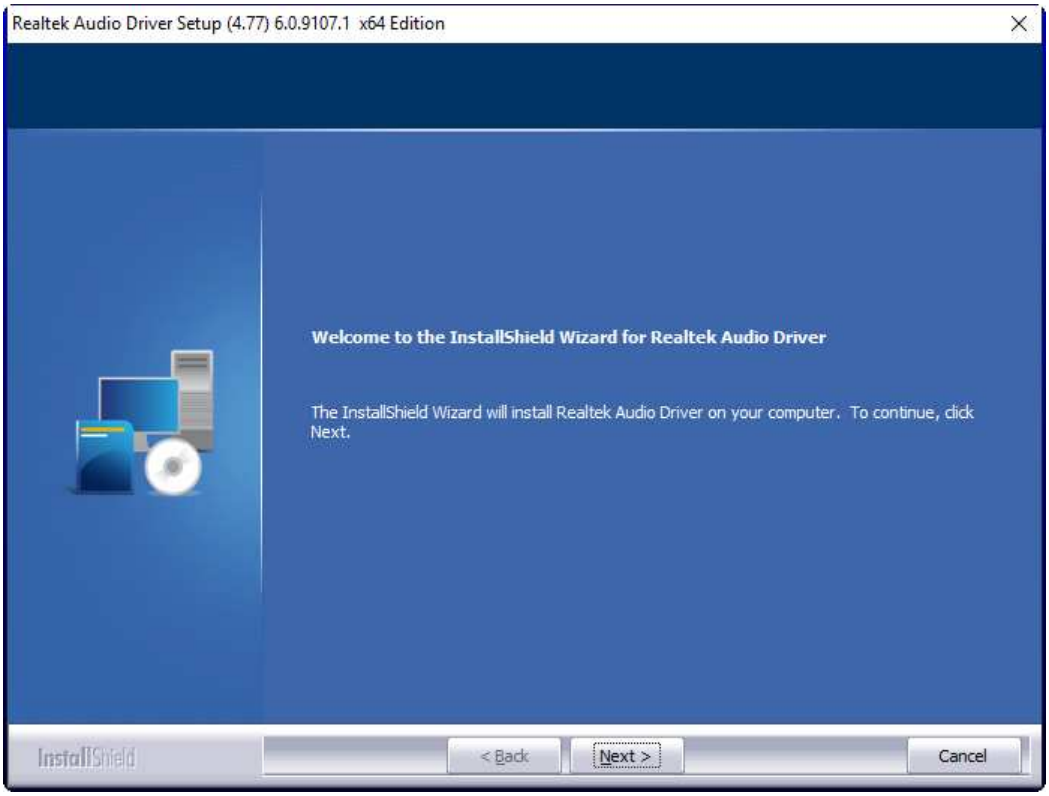
Step5. Select **Yes, I want to restart this computer now**. Click **Finish** to complete installation.



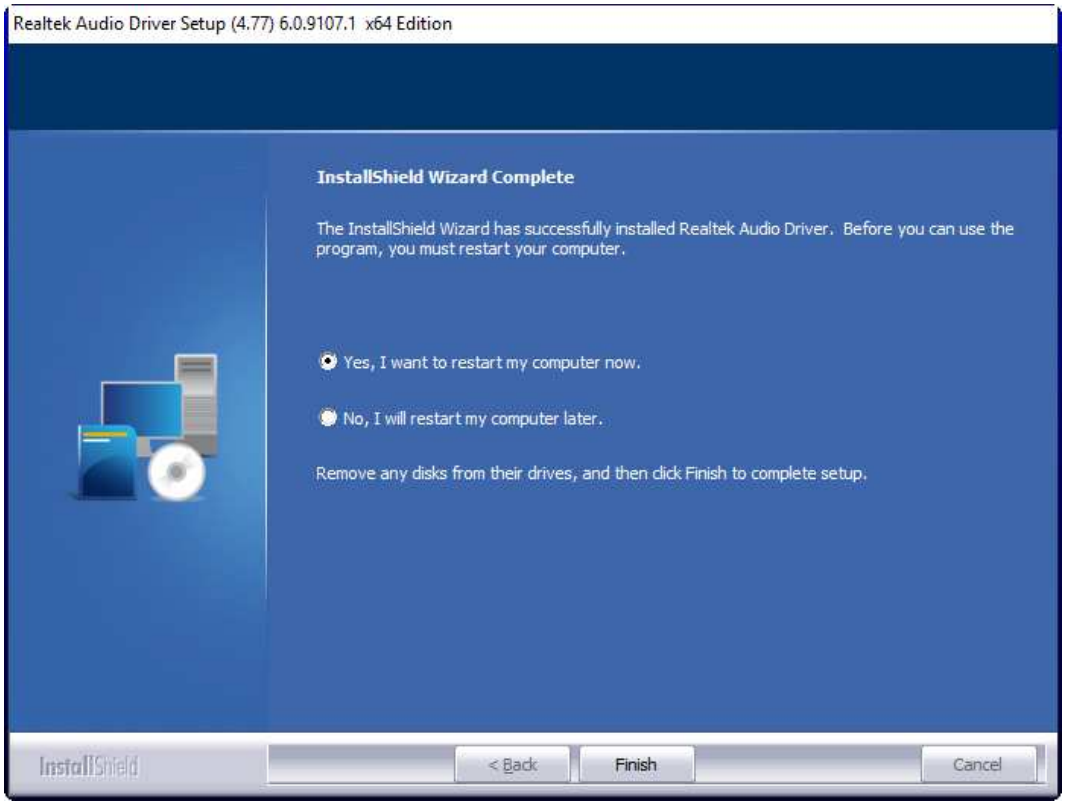
4.3 Realtek Audio Driver

To install the Realtek Audio Driver, please follow the steps below.

Step1. Select setup language you need. Click **Next** to continue.



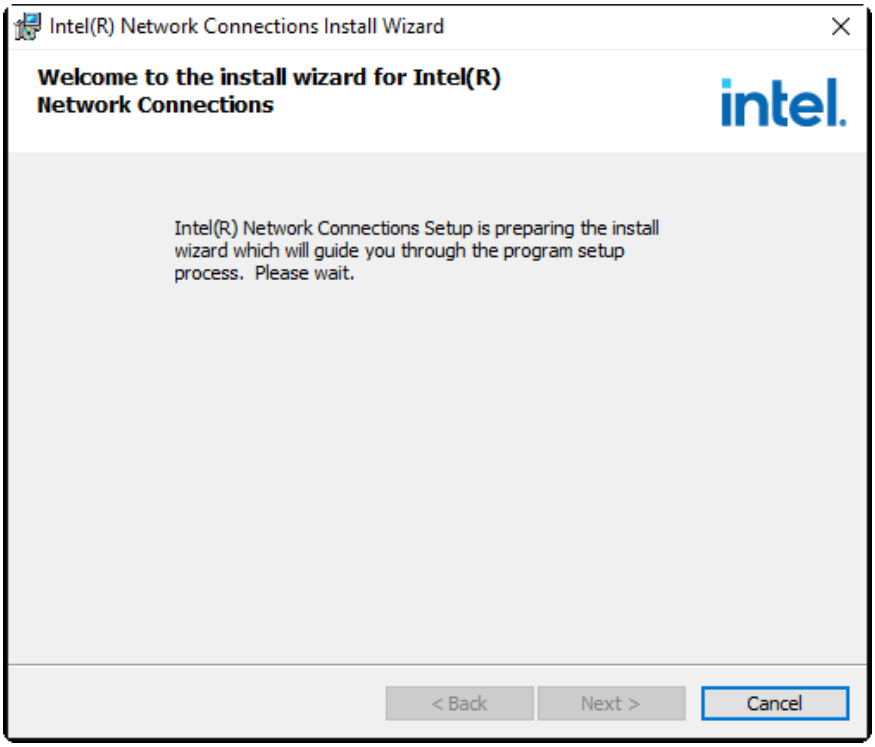
Step2. Click **Finish** to complete the installation.



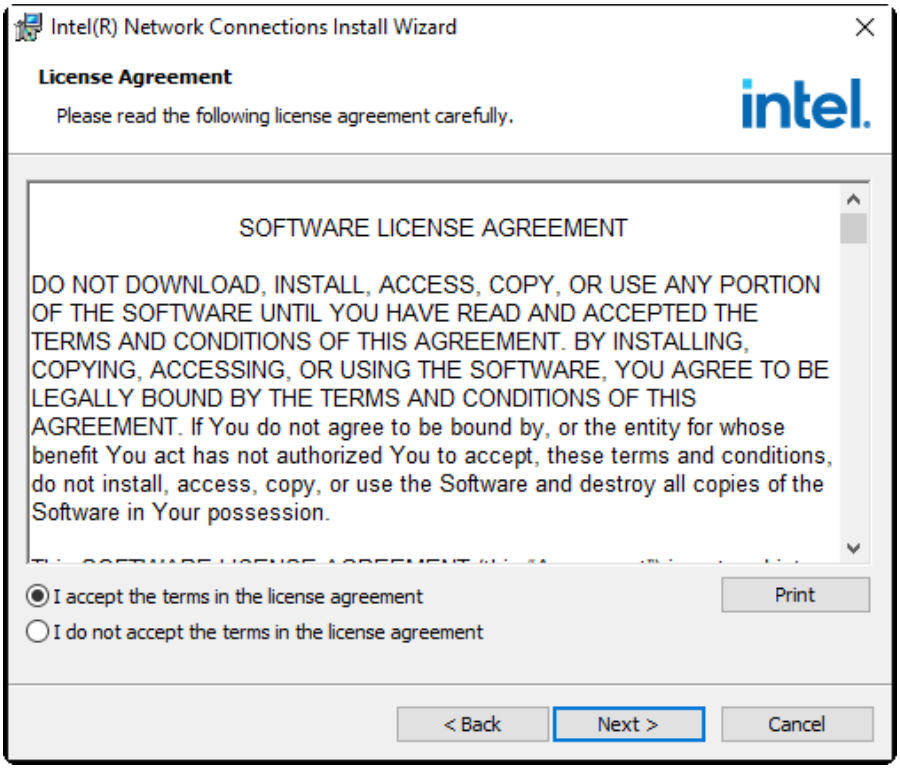
4.4 Intel® LAN Driver

To install the Intel® LAN Driver, please follow the steps below.

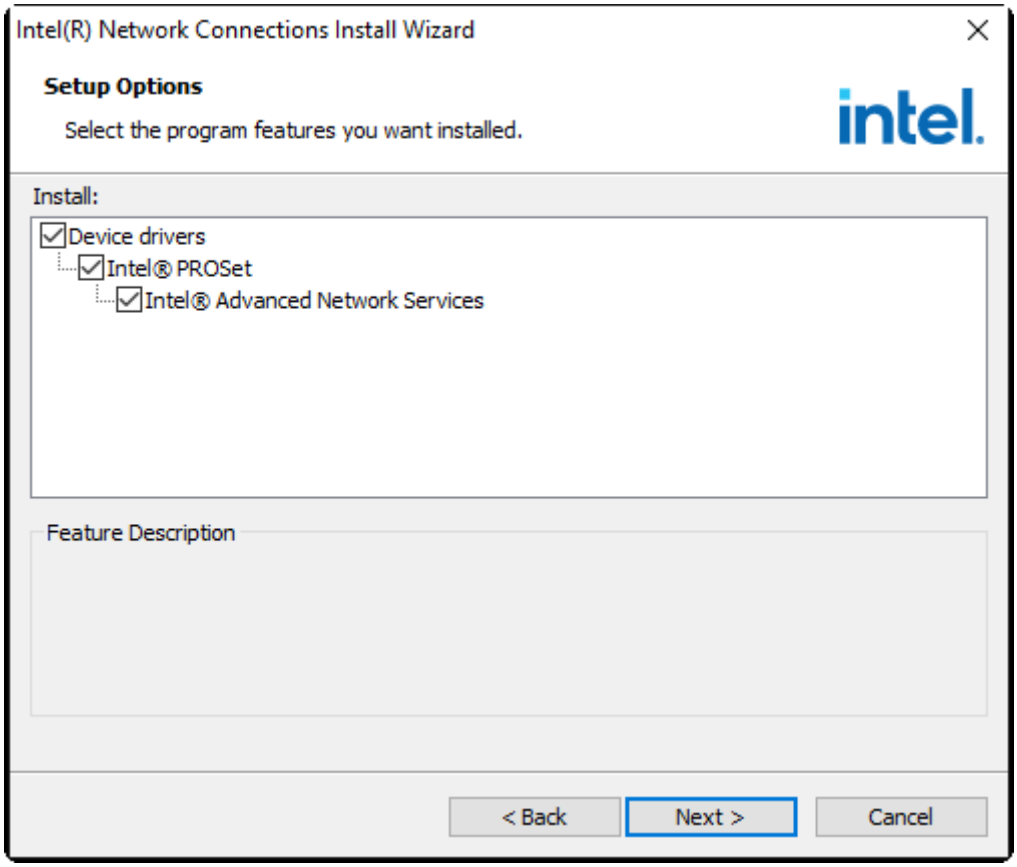
Step1. Here is welcome page. Please wait for program setup process.



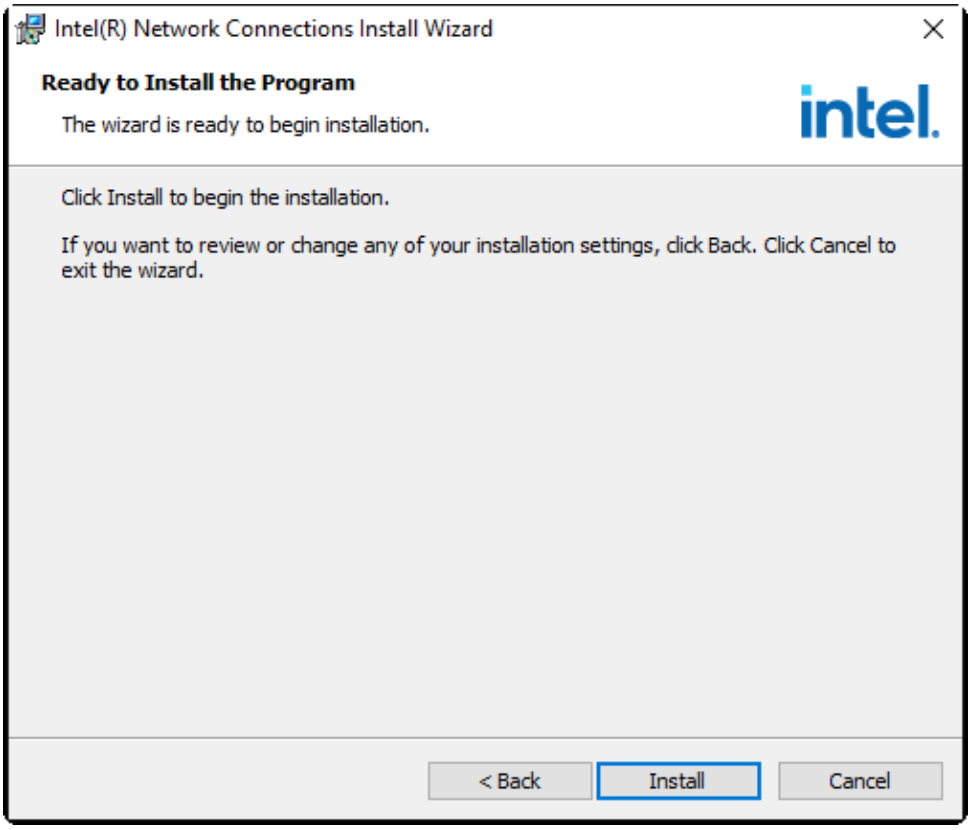
Step2. Read the license agreement. Select **I accept the terms in the license agreement** and click **Yes** to accept all of the terms of the license agreement.



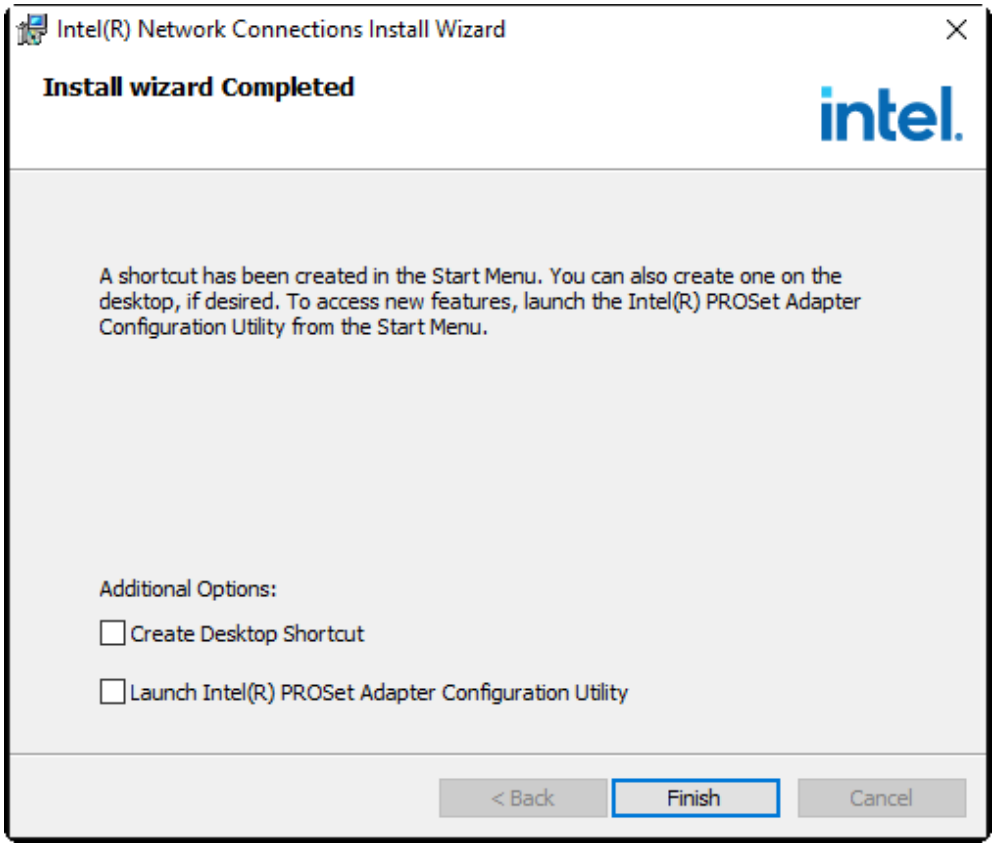
Step3. Click **Next** to continue.



Step4. Click **Install** to begin the installation.



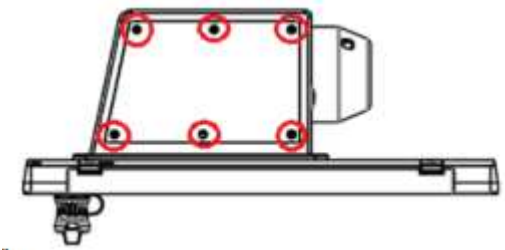
Step5. Click **Install** to begin the installation.



Chapter 5 Button Pin Setting

5.1 Loosen Swing ARM screws

Use screwdriver to loosen 6 pcs of screws at the side of the swing arm as pointed in picture below.



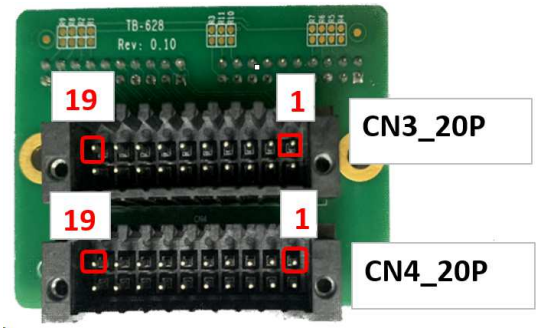
Note: After you have gained access to the push button extension boards, you can wire the push button extension.

5.2 Buttons Pin Setting

1-1 Take out the Terminal block 20-pin x2 units.

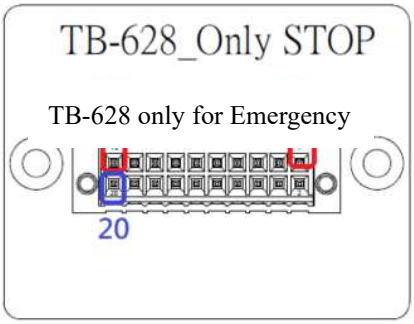
You can carry out the female connectors on the boards and connector the wiring with PLC when it is unplugged.

1-2 Set buttons' pin as definition below to connect to specified related system functions.



CN3_20P			
1	S8_N/O contact	2	S8_N/O contact
3	S8_N/C contact	4	S8_N/C contact
5	S8_LED(+24V)	6	S8_LED(GND)
7	S7_N/O contact	8	S7_N/O contact
8	S7_N/C contact	10	S7_N/C contact
11	S7_LED(+24V)	12	S7_LED(GND)
13	S6_N/O contact	14	S6_N/O contact
15	S6_N/C contact	16	S6_N/C contact
17	S6_LED(+24V)	18	S6_LED(GND)
19	S5_LED(+24V)	20	S5_LED(GND)

CN4_20P			
1	S5_N/O contact	2	S5_N/O contact
3	S5_N/C contact	4	S5_N/C contact
5	S4_N/O contact	6	S4_N/O contact
7	S4_N/C contact	8	S4_BN/C contact
8	S4_LED(+24V)	10	S4_LED(GND)
11	S3_N/O contact	12	S3_N/O contact
13	S3_N/C contact	14	S3_N/C contact
15	S3_LED(+24V)	16	S3_LED(GND)
17	S2_N/O contact	18	S2_N/O contact
19	NA	20	NA



TB-628_For Emergency_20P			
1	NA	2	NA
3	NA	4	NA
5	NA	6	NA
7	NA	8	NA
8	NA	10	NA
11	NA	12	NA
13	NA	14	NA
15	NA	16	NA
17	S1_COM2	18	S1_NC2
19	S1_COM1	20	S1_NC1

1-3 SThen the female connectors are plugged into the corresponding male connectors on the boards.

5.3 Fix screws back

After setting, fix the 6 pcs screws back on the swing arm with screwdriver.

Note: Excessive switching voltage may cause material damage.