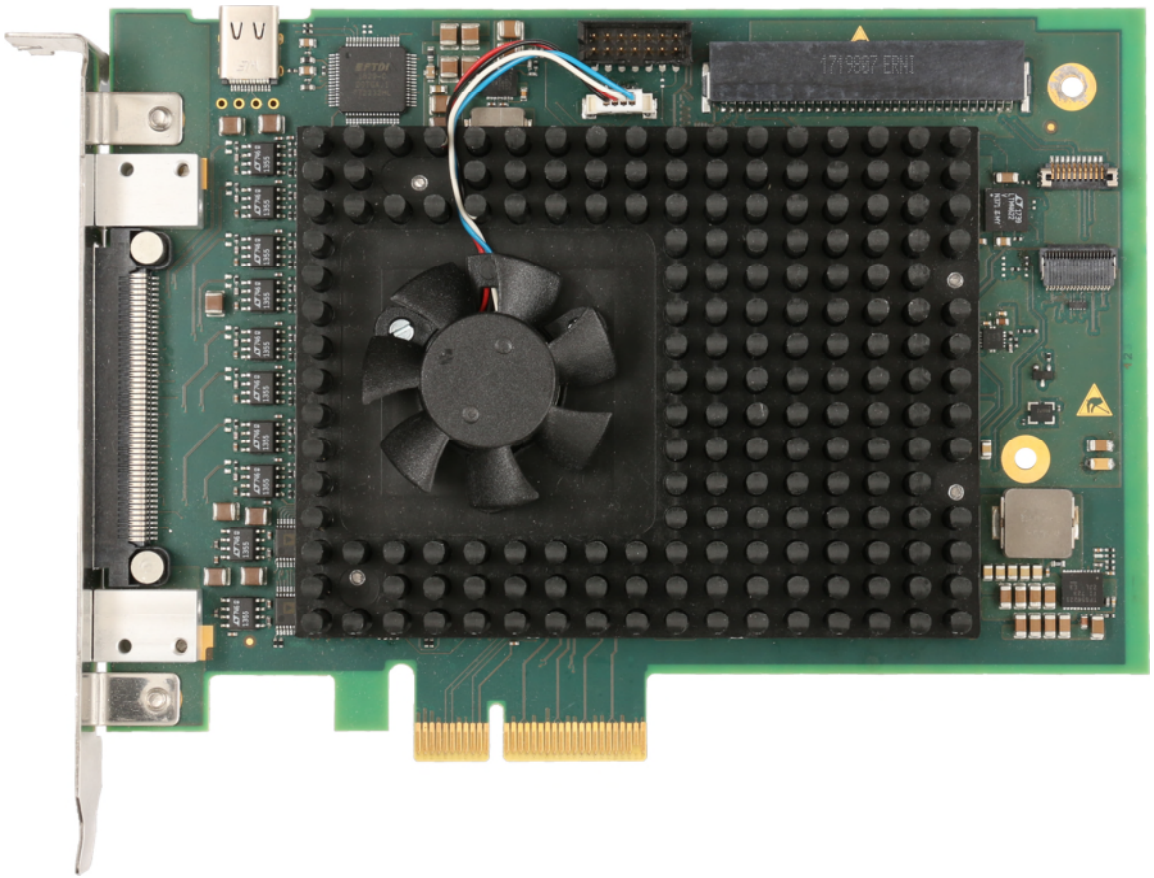
TPCE636 Reconfigurable FPGA with 16 x 16 bit Analog Input and 16 x 16 bit Analog Output



Application Information

The TPCE636 is a half-length X4 PCIe compatible module providing a user configurable Kintex7 FPGA with 16 ADC input channels and 16 DAC output channels.

The TPCE636 ADC input channels are based on the Linear Dual 16-Bit 5Msps Differential LTC2323-16 ADC. The TPCE636 provides 16 ADC channels. Each of the 16 channels has a resolution of 16bit and can work with up to 5Msps. The analog input circuit is designed to allow input voltages up to ±10V on each input-pin (results in ±20V differential voltage range).

The TPCE636 DAC output channels are based on the Dual 16bit AD5547 DAC. Each DAC output is designed as a single-ended bipolar ±10V analog output.

For customer specific I/O extension or inter-board communication, the TPCE636 provides 64 FPGA I/Os on a back I/O connector and 4 FPGA Multi-Gigabit-Transceiver on a Samtec FireFly© connector. Digital back I/O lines can be configured as 64 single ended LVCMOS25 or as 32 differential LVDS25 interface.

All front I/O lines such as the ADC interface and DAC interface are connected to a 98-pin. Samtec ERF8-049 Rugged EdgeRate Connector.

The User FPGA is connected to a 1GB, 32 bit wide DDR3 SDRAM. The SDRAM-interface uses an internal Memory Controller of the Kintex-7.

Issue 1.0.1
2019-03-19

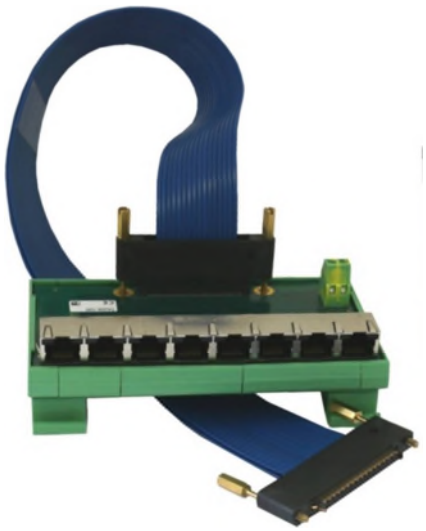
TEWS TECHNOLOGIES GmbH
Am Bahnhof 7 25469 Halstenbek, Germany
Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
e-mail: info@tews.com www.tews.com

The User FPGA is configured by a serial SPI flash. For full PCIe specification compliance, the XILINX Tandem Configuration Feature can be used for FPGA configuration. XILINX Tandem Methodologies "Tandem PROM" should be the favored Methodology. The SPI flash device is in-system programmable. An in-circuit debugging option is available via a JTAG header for read back and real-time debugging of the FPGA design (using Xilinx "ChipScope").

User applications for the TPCE636 with Kintex-7 FPGA can be developed using the design software Vivado Design Suite. A license for the Vivado Design Suite design tool is required.

TEWS offers a well-documented FPGA Board Reference Design. It includes constraint file with all necessary pin assignments and basic timing constraints. The FPGA Board Reference Design covers the main functionalities of the TPCE636.

The TPCE636 is delivered with the FPGA Board Reference Design. The user FPGA can be programmed via the on-board Board Configuration Controller (BCC). Programming via the JTAG interface using an XILINX USB programmer is also possible. In accordance with the PCI specification and the buffering of PCI header data, the contents of the user FPGA can be changed during operation.



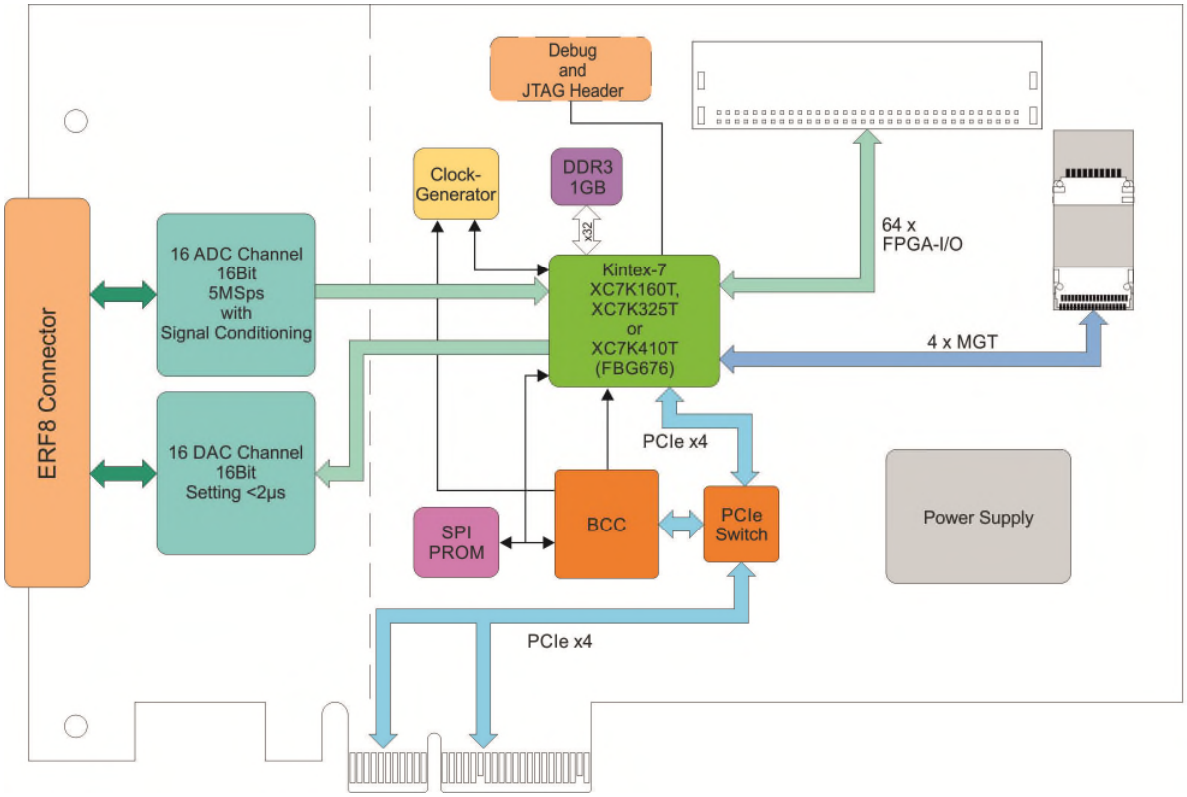
TA310

Technical Information

- Form Factor: half-length X4 PCIe
  - Board size: 153 mm x 98 mm
- PCI Express x4 Link (Base Specification 2.1) compliant interface conforming to ANSI/VITA 42.3-2006
- TPCE636 FPGA options:
  - -10R Xilinx XC7K160T-2FBG676I Kintex-7
  - -11R Xilinx XC7K325T-2FBG676I Kintex-7
  - -12R Xilinx XC7K410T-2FBG676I Kintex-7
- Serial Flash for FPGA Configuration
- FPGA clock options:
  - Local clock generator as source for the FPGA internal PLL
  - Free programmable Si514 Oscillator
- DDR3 SDRAM bank, 256M x 32 Bit (1GB)
- Front I/O lines
  - 16 differential analog inputs
    - 16 bit resolution
    - 5Msps
    - Factory calibration
  - 16 differential analog outputs
    - 16 bit resolution
    - max. ±10V single ended output
    - Factory calibration
- Back I/O lines
  - 64 single ended or 32 differential back I/O lines on a rear 68pin ERNI SMC connector.
  - 4 FPGA Multi-Gigabit-Transceiver on a rear Samtec FireFly(c) connector.
- Operating temperature -40°C to +85°C
- MTBF (MIL-HDBK217F/FN2 GB 20°C): 240000h

Issue 1.0.1
2019-03-19

TEWS TECHNOLOGIES GmbH
Am Bahnhof 7 25469 Halstenbek, Germany
Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
e-mail: info@tews.com www.tews.com



Block Diagram TPCE636

Order Information

RoHS Compliant

TPCE636-10R	Kintex-7 FPGA 1GBDDR3	XC7K160T-2	FBG676,	16 x Analog In, 16 x Analog Out and 64 direct FPGA Back I/O Lines, 4 MGTs on FireFly connector ©
TPCE636-11R	Kintex-7 FPGA 1GBDDR3	XC7K325T-2	FBG676,	16 x Analog In, 16 x Analog Out and 64 direct FPGA Back I/O Lines, 4 MGTs on FireFly connector ©
TPCE636-12R	Kintex-7 FPGA 1GBDDR3	XC7K410T-2	FBG676,	16 x Analog In, 16 x Analog Out and 64 direct FPGA Back I/O Lines, 4 MGTs on FireFly connector ©

Documentation

TPCE636-DOC	User Manual

Software

TDRV018-SW-25	Integrity Software Support
TDRV018-SW-42	VxWorks Software Support (Legacy and VxBus-Enabled Software Support)
TDRV018-SW-65	Windows Software Support
TDRV018-SW-82	Linux Software Support
TDRV018-SW-95	QNX Software Support

For other operating systems please contact TEWS.

Related Products

TA310	Cable Kit for Modules with Samtec ERF8-049-Connector